PM7350

S/UNI™-DUPLEX

DSLAM

REFERENCE DESIGN

LINE CARD

RELEASED

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PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Apr 1999	Document created.
2	Aug 1999	Changed name from S/UNI-DUPLEX Reference Design to DSLAM Reference Design: Line Card. Added register configurations. Added FPGA Design. Added schematics. Revised description of timing distribution.
3	Nov 2000	Changed status to Released. Added Layout. Back-annotated schematics. Added Bill of Materials. Added FPGA Code. Revised COMET register configuration.

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1 DEFINITIONS

ADSL	Asymmetric Digital Subscriber Line
ATM	Asynchronous Transfer Mode
CABGA	Chip Array Ball Grid Array
CO	Central Office
COMET	PMC-Sierra's mnemonic for the PM4351 Combined E1/T1 Framer/Transceiver
DSLAM	Digital Subscriber Line Access Multiplexer
LAN	Local Area Network
LVDS	Low Voltage Differential Signal
PBGA	Plastic Ball Grid Array
POTS	Plain Old Telephone Service
PSTN	Public Switched Telephone Network
S/UNI	SATURN User Network Interface
S/UNI-APEX	PMC-Sierra's mnemonic for the PM7326 ATM/PACKET Traffic Manager and Switch
S/UNI-DUPLEX	PMC-Sierra's mnemonic for the PM7350 Dual Port Serialized UTOPIA Multiplexer
S/UNI-VORTEX	PMC-Sierra's mnemonic for the PM7351 Eight Port Serialized UTOPIA Multiplexer
WAN	Wide Area Network

2 FEATURES

- A reference design of the Line Card portion of a DSLAM system.
- Showcases a high-density architecture with the PBGA S/UNI-DUPLEX and CABGA COMET devices.
- Supports 16 serial interfaces to transport ATM over T1/E1.
- Contains short-haul (intra-building) protection circuitry for high-speed telecommunication lines.
- A high-speed LVDS Interface capable of data rates up to 200 MB/s.
- Supports 1:1 protection switching to a Core Card.
- Allows clock synchronization through the use of an embedded reference clock.
- A serial interface to the onboard microprocessor to configure, control and monitor the S/UNI-DUPLEX and COMET devices.
- An embedded inter-device communications channel, allowing devices on the Core Card to communicate with devices on the Line Card.
- Supports hot swap capability to allow live insertion/extraction.
- CompactPCI (cPCI) compatible.

3 REFERENCES

1. PCI Industrial Computers Manufacturers Group (PICMG), “CompactPCI Specification 2.0 R 2.1”, Wakefield MA, September 1997.

2. PMC-Sierra Inc., PMC-1970624, “COMET - Combined E1/T1 Transceiver/Framer Long Form Data Sheet”, July 1999, Issue 8.

3. PMC-Sierra Inc., PMC-1981025, “S/UNI-VORTEX and S/UNI-DUPLEX Technical Overview”, June 1999, Issue 2.

4. PMC-Sierra Inc., PMC-1980581, “S/UNI-DUPLEX Dual Serial Link PHY Multiplexer Data Sheet”, April 2000, Issue 5.

5. PMC-Sierra Inc., PMC-1990832, “DSLAM Reference Design: System Design”, September 2000, Issue 3.

6. PMC-Sierra Inc., PMC-1990815, “DSLAM Reference Design: Core Card”, September 2000, Issue 3.

7. PMC-Sierra Inc., PMC-1990474, “DSLAM Reference Design: WAN Card”, September 2000, Issue 3.

4 SCOPE

The purpose of this reference design is to assist engineers in designing their products using PMC-Sierra's S/UNI-DUPLEX device.

The DSLAM Reference Design is composed of the following four documents:

- DSLAM Reference Design: System Design
- DSLAM Reference Design: Core Card
- DSLAM Reference Design: Line Card
- DSLAM Reference Design: WAN Card

The DSLAM Reference Design: System Design document provides an overview of the DSLAM system architecture. The remaining documents describe the functionality and implementation specific details for each individual card.

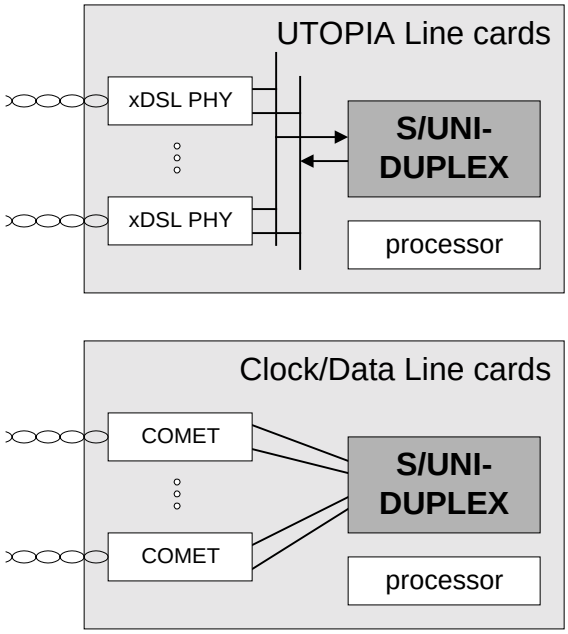
This document only describes designs for the DSLAM Line Card based on the S/UNI-DUPLEX device. A block diagram is shown for the design. A description is then given for the functional blocks of the design. A detailed implementation description then follows.

5 BLOCK DIAGRAM

5.1 S/UNI-DUPLEX Architecture

The S/UNI-DUPLEX provides a SCI-PHY/Any-PHY interface or a clocked serial data interface. The use of the SCI-PHY/Any-PHY interface and the clocked serial data interface is mutually exclusive due to the fact that many signals of these two interfaces share physical package pins. Therefore, it is this interface that defines the architecture of the Line Card. Figure 1 shows the two possible Line Card architectures based on the PHY/FRAMER interfaces.

Figure 1 - DSLAM Line Card Architectures



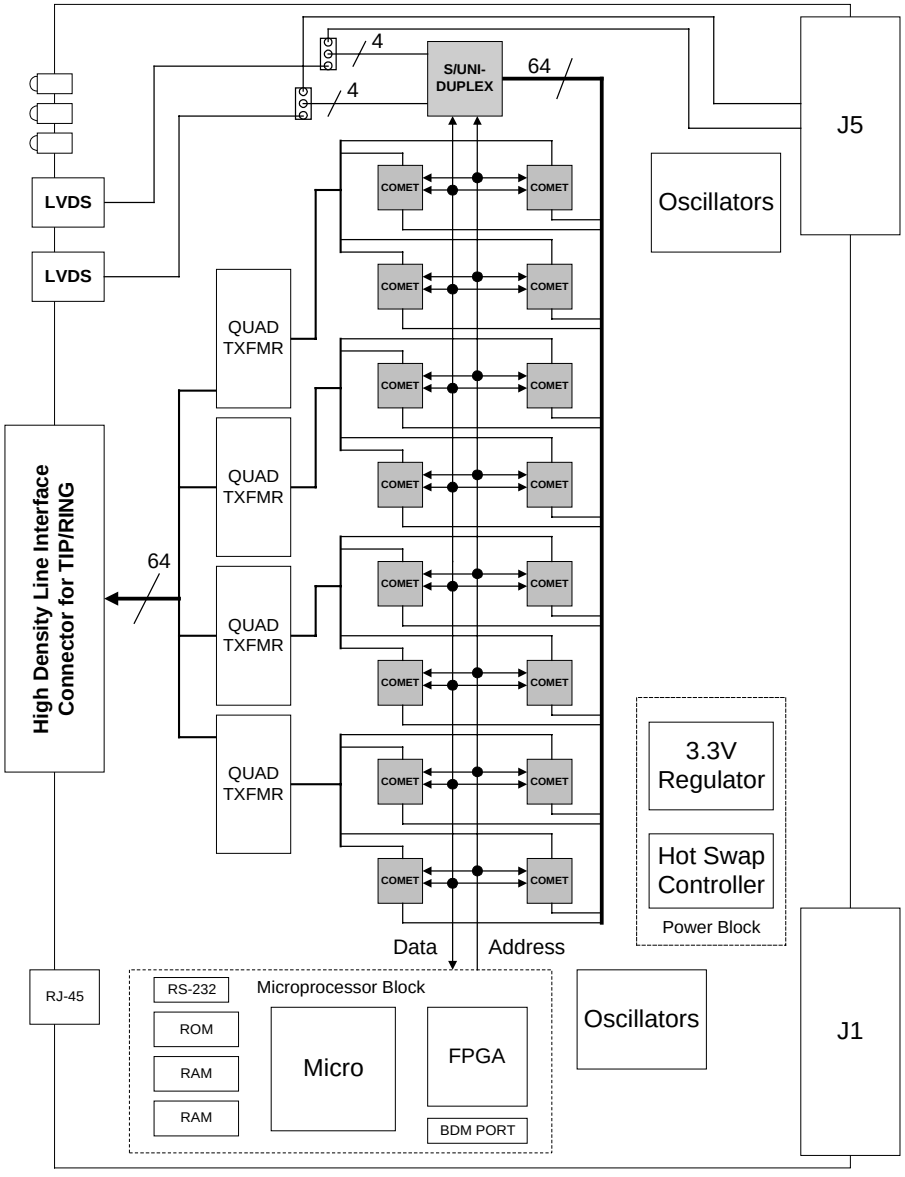
This reference design is based on the serial clock and data architecture. An example of the UTOPIA bus architecture is left for the DSLAM Reference Design: WAN Card [8].

5.2 S/UNI-DUPLEX Line Card

A block diagram for this design is shown in Figure 2. For upstream traffic, a high-density connector transports 16 T1/E1 lines onto the board. The 16 T1/E1 line inputs are connected to 16 COMET devices. The clock and data lines from each COMET are then connected to the S/UNI-DUPLEX. The S/UNI-DUPLEX takes the clocked serial data and multiplexes the data onto the high-speed LVDS

interface. This high-speed LVDS interface transports data to the Core Card. For downstream traffic, the Core Card transmits data for the 16 physical interfaces through the high-speed LVDS interface. The S/UNI-DUPLEX receives the LVDS data and demultiplexes the LVDS data. It is then sent to the COMET for transmission over the T1/E1 interface.

Figure 2 - DSLAM Line Card Block Diagram



This design illustrates the S/UNI-DUPLEX interface for clocked serial data. Full serial fan-in potential of the S/UNI-DUPLEX device is demonstrated.

6 FUNCTIONAL DESCRIPTION

The following sections describe the functional blocks of the block diagram shown in Figure 2.

6.1 S/UNI-DUPLEX

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit typically used for traffic concentration within a Digital Subscriber Line Access Multiplexer (DSLAM).

The device is ATM specific. It exchanges contiguous 53 byte cells with PHY devices. The PHY interface can be either clocked serial data or SCI-PHY/Any-PHY.

With a clocked serial data configuration up to sixteen channels are supported. Cell alignment is established through HCS (Header Check Sequence) delineation. The cell payload is scrambled and descrambled with a $x^{43} + 1$ polynomial. Rate adaptation is performed through idle cell insertion and extraction. Each PHY interface has a dedicated four cell FIFO in both upstream and downstream directions.

All cell streams are multiplexed into a high-speed serial stream. The high-speed interfaces use NRZ data-only differential signals compatible with LVDS levels. The internal transmit clock is synthesized from a lower frequency reference. An extended cell format provides four extra bytes for the encoding of flow control, timing reference, PHY identification and link maintenance information. A redundant link is provided to allow connection to two cell processing cards.

A microprocessor port provides access to internal configuration and monitoring registers. The port may also be used to insert and extract cells in support of a control channel.

For further information, please see the S/UNI-DUPLEX Datasheet PMC-1980581 [5].

6.2 COMET

The PM4351 Combined E1/T1 Transceiver (COMET) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1 and E1 systems with a minimum of external circuitry. The COMET is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 43 dB cable loss (at 1.024 MHz in E1 mode) or up

to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digital line inputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to several DS-1 signal formats: SF, ESF, T1DM (DDS) and SLC®96. In E1 mode, the COMET frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET also supports reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET integrates Red and AIS alarms.

In T1 mode, the COMET generates framing for SF, ESF and T1DM (DDS) formats. In E1 mode, the COMET generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements. Digital line inputs and outputs are provided for applications not requiring a physical T1 or E1 interface.

In the transmit path, the COMET supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side

data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET provides optional jitter attenuation in both the transmit and receive directions.

The COMET provides both a parallel microprocessor interface for controlling the operation of the device and serial PCM interfaces that allow backplane rates from 1.544 Mbit/s to 8.192 Mbit/s to be directly supported.

For further information, please see the COMET Datasheet PMC-1970624 [3].

6.3 Microprocessor Block

An on-board microprocessor is used to monitor and control the S/UNI-DUPLEX and COMET devices. It requires the following features:

- 8-bit data bus
- Address bus
- Programmable chip selects
- Interrupt controller
- Serial interface
- Background Debug Module

The MC68340 was chosen for this reference design.

An FPGA is used in the microprocessor block to provide the glue logic necessary to interface MC68340 to the PMC-Sierra devices. The FPGA will provide address decoding to generate the chip selects to all the PMC-Sierra devices. The FPGA will also be used as a buffer to balance the load on the address and data busses. The VHDL code for the FPGA is included in Appendix C.

6.4 Timing

The timing block consists of the oscillators and part of the FPGA. Timing on the Line Card requires providing clock signals to 18 devices on the board: one S/UNI-DUPLEX, 16 COMETs and one MC68340.

The MC68340 requires two oscillators. A 25 MHz clock is needed for the processing core. A 3.6864 MHz clock is needed for the serial interface. On-board oscillators provide these timing sources.

The S/UNI-DUPLEX requires one jitter-free clock input for REFCLK. It is used as the reference clock by both clock recovery and clock synthesis circuits. The high-speed serial interface bit rate is eight times the REFCLK frequency. A 25 MHz on-board oscillator is used for this input.

Each COMET requires a jitter-free clock input for XCLK to provide timing for internal circuitry. An on-board 2.048 MHz oscillator provides the XCLK input.

The FPGA is used to distribute an 8 kHz reference clock. This reference timing for the PMC-Sierra devices is used to clock data throughout the system. Please refer to the DSLAM Reference Design: System Design [6] document for a thorough discussion on the use of the reference clock.

6.5 Power Block

Power requirements of the board are +5V and +3.3V. +5V is available through J1 of the CompactPCI backplane. A linear regulator is used to regulate +3.3V from the +5V supply. Front panel LEDs will be used to indicate power status.

A hot swap controller is used to manage the power of the board during insertion and removal.

6.6 Connectors

There are two groups of connectors for the Line Card: the faceplate connectors and the backplane connectors. The faceplate connectors consist of the LVDS connectors, T1/E1 connector and the microprocessor serial interface connector. The backplane connectors are CPCI connectors J1 and J5.

The LVDS connector requires a bandwidth of 100 to 200 Mb/s. The IEEE 1394 Firewire plug was chosen to meet both the bandwidth and board space requirements. It is used to carry the LVDS data from the Line Card to the Core Card over Firewire cables.

The physical limitations of the CompactPCI board does not allow 16 T1/E1 transmit/receive interfaces to be placed in an accessible fashion on the front panel. Therefore, a high-density connector to accommodate the line interfaces is used. These can easily be moved to a rear I/O card on the rear of the CompactPCI shelf with the signals going through the CompactPCI backplane connectors. However, this would require a rear I/O board to be designed and manufactured and therefore is not included in this reference design.

The microprocessor serial interface connector is a RJ-45 style connector. It is used to communicate with the microprocessor through a simple serial interface such as a dumb terminal or Windows HyperTerminal.

J1 is used to supply power and ground to the board only. All digital signals from the CPCI motherboard are left unconnected. J5 is used to transport the LVDS data from the Line Card to the Core Card over a backplane. This is an option of the Line Card and is configured through jumpers on the board.

7 IMPLEMENTATION DESCRIPTION

The following sections describe detailed design considerations of the reference design.

7.1 S/UNI-DUPLEX Design Considerations

7.1.1 SCIANY Pin

The SCI-PHY/Any-PHY Interface (SCIANY) input selects the type of PHY device interface. To configure the S/UNI-DUPLEX for clocked serial data, this pin must be a logic low.

7.1.2 Register Configuration

On power-up or reset, the S/UNI-DUPLEX registers are reset to the default setting as described in the datasheet [5]. Table 1 shows the registers changed after reset.

Table 1 - S/UNI-DUPLEX Register Configuration

Register	Power-up Default	Firmware Default	Description
0x01h Master Configuration	0x02h	0x26h	LTXCINV = 1 Configures the serial data to update the TX on the falling edge of the clock. MINTE = 1 Turns on Master Interrupt Enable bit.
0x5Eh Transmit Logical Channel FIFO Depth	0x00h	0x04h	FDEPTH[5:0] = 000100b For the Clocked Serial Data Interface, this FIFO depth is needed for correct operation.

Further configuration of the S/UNI-DUPLEX can be accomplished via the serial interface of the microprocessor.

7.1.3 Power Supply

During power-up, the BIAS pin must be equal to or greater than the voltage on the VDD pins. This is accomplished with the voltage regulator. The voltage on the BIAS pin is also the same one used to regulate the VDD voltage. Therefore, the worst case is that the regulator malfunctions and shorts, which still leaves the BIAS pin equal to VDD. Also, an extra protection diode is used to limit the VDD to a maximum of 0.5V above the BIAS voltage.

Analog power pins QAVD, CAVD, RAVD and TAVD must be applied after VDD or they must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between VDD and the AVD pin to delay the power to the AVD pin.

The differential voltage measured between AVD supplies and VDD must be less than 0.5V.

7.1.4 Decoupling

A 0.01µF or 0.1µF capacitor is placed between power and ground for each VDD pin. The capacitor should be placed as close to the actual pin as possible.

The AVD pins require a filtering network between the VDD supply and each AVD pin. The network is a single RC network with the resistor between the VDD supply and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics in Appendix A for component values.

7.1.5 Octet Alignment

The S/UNI-DUPLEX is configured for a bit-aligned interface with the COMET. This allows a glueless interface between the S/UNI-DUPLEX and COMET. To implement an octet-aligned interface with the COMET, the ALIGN bit must be set to 1 in Register 0x74: Transmit Serial Alignment Control. This configures the S/UNI-DUPLEX to output the most significant bit of the data octet during the gap period. LTXD[N] will then need to be delayed by one clock cycle in order to align the most significant bit of the octet to output as the first bit after the gap period. This can be accomplished by placing flip-flop into the data path to hold the data by one clock cycle.

7.2 COMET Design Considerations

7.2.1 Register Configuration

On power-up or reset, the COMET registers are reset to the default setting as described in the datasheet [3]. Table 2 shows the registers changed after reset.

Table 2 - COMET Register Configuration

Register	Power-up Default	Programmed Value	Description of changes
0x0F2h XLPG Pulse Waveform Storage Write Address	0x00h	see Datasheet	The XLPG registers are modified for transmit waveform values corresponding to T1 Short Haul (0 – 110ft.).
0x0F3h XLPG Pulse Waveform Storage Data	0x00h	see Datasheet	
0x000h Global Configuration	0x80h	0x10h	Sets the PIO pin as input. Sets the RSYNC to use digital loss of signal. Sets the COMET devices to operate in T1 mode.
0x0F0 XLPG Line Driver Configuration	0x80h	0x0Ch	Enables the XLPG and sets the SCALE[4..0] bits for T1 Short Haul (0 – 110ft.)
0x0D6 CSU Configuration	0x00h	0x07h	Sets XCLK = 2.048MHz, TCLKO = 1.544MHz
0x01C RX-ELST Configuration	0x03h	0x00h	Configures for T1 mode.
0x020 TX-ELST Configuration	0x03h	0x00h	Configures for T1 mode.
0x048 T1 FRMR Configuration	0x00h	0x30h	Enables ESF framing.
0x054 T1 XBAS Configuration	0x00h	0x30h	Enables ESF framing and B8ZS Line Encoding.
0x060 T1 ALMI Configuration	0x00h	0x10h	Enables ESF framing.
0x050 SIGX Configuration	0x00h	0x04h	Enables ESF framing.

Register	Power-up Default	Programmed Value	Description of changes
0x030 BRIF Configuration	0x38h	0x00h	BRCLK is configured to be an output. BRPCM is updated on the falling edge.
0x031 BRIF Frame Pulse Configuration	0x20h	0x00h	Sets BTFP as frame pulse master.
0x032 BRIF Parity	0x00h	0x01h	Enables backplane data and signaling
0x0FF RLPS Equalizer Configuration	0x03h	0x0Bh	Enables Equalizer Feedback Loop.
0x002 Receive Options	0x80h	0x00h	Enables RJAT.
0x0DC RLPS Equalizer Voltage Reference	0x00h	0x2Ch	Sets the voltage reference of the analog receive equalizer.
0x0D8-0x0DB and 0x0FD-0x0FC Receive Equalizer Table	0x00h	see Datasheet	The RLPS equalization table is set for T1.

Further configuration of the COMET can be accomplished via the serial interface of the microprocessor.

7.2.2 Power Supply

During power-up, the BIAS pin must be equal to or greater than the voltage on the VDD pins. This is accomplished with the voltage regulator. The voltage on the BIAS pin is also the same one used to regulate the VDD voltage. Therefore, the worst case is that the regulator malfunctions and shorts, which still leaves the BIAS pin equal to VDD. Also, an extra protection diode is used to limit the VDD to a maximum of 0.5V above the BIAS voltage.

Analog power pins must be applied after VDD or they must be current limited to the maximum latch-up current of 100mA. A simple solution is to use a small filtering network between VDD and the AVD pin to delay the power to the AVD pin.

The differential voltage measured between AVD supplies and VDD must be less than 0.5V.

7.2.3 Decoupling

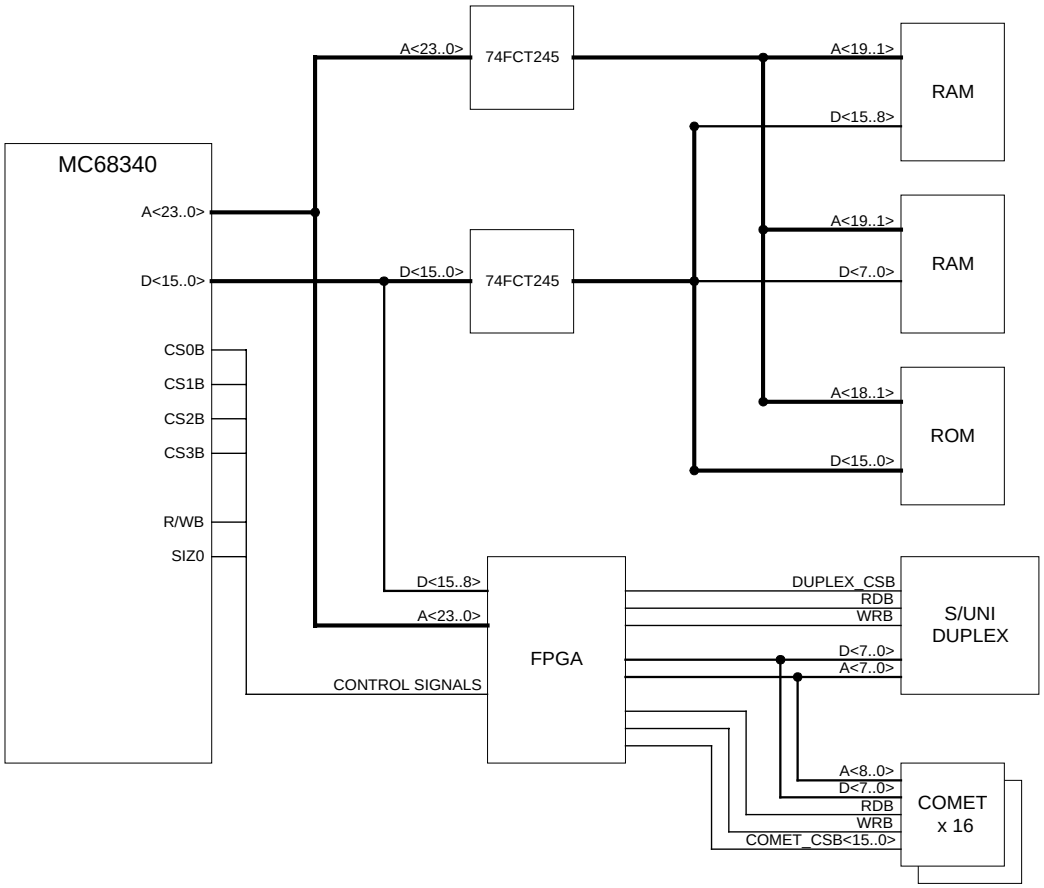
A 0.01µF capacitor is placed between power and ground for the VDDO pins. A 0.1µF capacitor is placed between power and ground for the VDDI pins. The capacitors should be placed as close to the actual pin as possible.

The AVD pins require a filtering network between the VDD supply and each AVD pin. The network is a single RC network with the resistor between the VDD supply and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to the schematics in Appendix A for component values.

7.3 Microprocessor Interface

Figure 3 shows a block diagram of the microprocessor block and its interface with the PMC-Sierra devices.

Figure 3 - Microprocessor Block Diagram



The MC68340 signals used to generate the chip select bits for the PMC-Sierra devices are CS2B and A<23..0>. The chip select logic is performed in the FPGA. The FPGA also provides a RDB and a WRB to the PMC-Sierra devices generated from R/WB of the microprocessor. Other control signals from the microprocessor are used to generate control signals for the RAM, ROM and debug port. The VHDL code for the FPGA is included in Appendix C.

7.4 Reference Timing Distribution

The S/UNI-DUPLEX provides a method of transporting a reference clock over the LVDS connection. By using the TX8K and RX8K pins of the S/UNI-DUPLEX, a low speed reference clock can be sent or received respectively. This reference clock is typically an 8 kHz clock used for timing PCM voice circuitry. However, the reference clock is not constrained to 8 kHz, any frequency less than the cell rate is permissible.

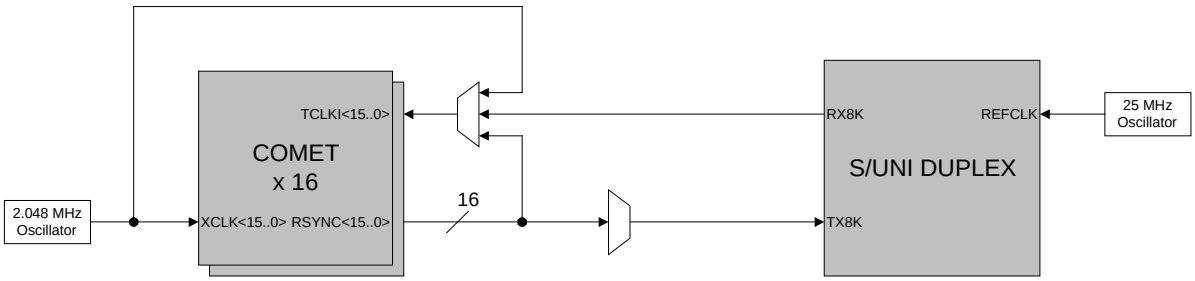
The rising edge of TX8K initializes an internal counter to count the number of bytes in the high-speed serial cell being sent over the LVDS connection. The counter is encoded into the TREF[5..0] bits of the System Prepend Bytes of the LVDS ATM cell. An all ones value indicates no timing mark is associated with this cell. On the receiver side, the inherent jitter is at ± one octet. For example, at 155 MHz, the jitter is ± 52 ns, at 200 MHz it is ± 40 ns.

For a discussion on system timing, please refer to the DSLAM Reference Design: System Design [6] document.

7.5 FPGA Design

In this design, the FPGA is used to distribute an 8 kHz reference clock to devices on the board based on internal registers programmed into the FPGA. Figure 4 shows the different timing options available and the multiplexing performed by the FPGA.

Figure 4 - 8kHz Timing Options



The following registers are available on the FPGA: 0x00h-0x01h COMET TCLK Selection and 0x02h S/UNI-DUPLEX TX8K Selection.

Table 3 - COMET TCLK Selection (0x00h – 0x01h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Unused	C[5]	C[4]	C[3]	C[2]	C[1]

Register 0x00h – 0x01h selects the TCLK input for COMET #0 to COMET #7 and COMET #8 to COMET #15 respectively. Table 4 shows the use of the C[5..1] bits. Default for both TCLK Selection Registers are “10000”, 2.048 MHz oscillator.

Table 4 - Clock Source select bits

C[5..0]	Clock Source Selected
00000	COMET #0 RSYNC
00001	COMET #1 RSYNC
00010	COMET #2 RSYNC
00011	COMET #3 RSYNC
00100	COMET #4 RSYNC
00101	COMET #5 RSYNC
00110	COMET #6 RSYNC
00111	COMET #7 RSYNC
01000	COMET #8 RSYNC
01001	COMET #9 RSYNC
01010	COMET #10 RSYNC
01011	COMET #11 RSYNC
01100	COMET #12 RSYNC
01101	COMET #13 RSYNC
01110	COMET #14 RSYNC
01111	COMET #15 RSYNC
10000	2.048 MHz Oscillator
11111	S/UNI-DUPLEX RX8K

Table 5 - S/UNI-DUPLEX TX8K Selection (0x02h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Unused	Unused	C[4]	C[3]	C[2]	C[1]

Register 0x02h S/UNI-DUPLEX TX8K input selects the source for the TX8K pin of the S/UNI-DUPLEX. Table 6 shows the use of the C[4..1] bits. The default is “0000”, COMET #0 RSYNC.

Table 6 - Clock Source select bits

C[4..0]	Clock Source Selected
0000	COMET #0 RSYNC
0001	COMET #1 RSYNC
0010	COMET #2 RSYNC
0011	COMET #3 RSYNC
0100	COMET #4 RSYNC
0101	COMET #5 RSYNC
0110	COMET #6 RSYNC
0111	COMET #7 RSYNC
1000	COMET #8 RSYNC
1001	COMET #9 RSYNC
1010	COMET #10 RSYNC
1011	COMET #11 RSYNC
1100	COMET #12 RSYNC
1101	COMET #13 RSYNC
1110	COMET #14 RSYNC
1111	COMET #15 RSYNC

The FPGA also has the ability to control the COMET status LEDs. Table 7 shows register 0x03h of the FPGA.

Table 7 - COMET Status LEDs (0x03h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused	Unused	Unused	Unused	C 1-4	C 5-8	C 9-12	C 13-16

The front panel LEDs are lit if the corresponding bit of the LED is set to “1”.

7.6 LED Description

There are three sets of LEDs for the Line Card.

The basic set of LEDs provides visual information about power and the microprocessor.

- +5 V, green – indicates presence of +5 V
- +3.3 V, green – indicates presence of +3.3 V
- uP, green – ON indicates trouble at uP (power-up boot) or RESET
- Heart Beat, green – indicates healthy uP interface to all components

Additional red LEDs indicate loss of signal and loss of cell delineation on the S/UNI-DUPLEX.

- LOS1, red – loss of signal at LVDS RXD1
- LCD1, red – loss of cell delineation at LVDS RXD1
- LOS2, red – loss of signal at LVDS RXD2
- LCD2, red – loss of cell delineation at LVDS RXD2

LED indication loss of signal and loss of frame on the COMET devices are grouped by four.

- C 1-4, red – loss of signal or frame at COMET 1 to 4
- C 5-8, red – loss of signal or frame at COMET 5 to 8
- C 9-12, red – loss of signal or frame at COMET 9 to 12
- C 13-16, red – loss of signal or frame at COMET 13 to 16

7.7 Jumper Configuration

There are two sets of jumpers on the board: LVDS and microprocessor.

The LVDS jumpers are used to manually select the LVDS datapath. The LVDS can be configured to communicate through the front panel connectors or the backplane connectors.

The microprocessor jumpers are used to manually select whether the microprocessor runs from ROM or from the BDM port.

7.8 Hot Swap Design Notes

When a board is plugged into a backplane, large transient currents can be drawn to charge up the bypass capacitors on the board. This can cause the voltage from the power supply to dip. The dip in voltage levels can cause other boards in the system to fail. Also, the connector pins may be damaged because they are not able to handle the large currents.

The solution is to use an N-channel MOSFET transistor to ramp up the supply voltage in a controlled manner. A hot swap controller, the LTC1422 in this design, can be used to control the gate of the N-channel transistor. By ramping the voltage at a controlled rate, the transient surge current

$$I = C * \frac{dV}{dt}$$

is controlled and limited to a safe value when the board makes connection.

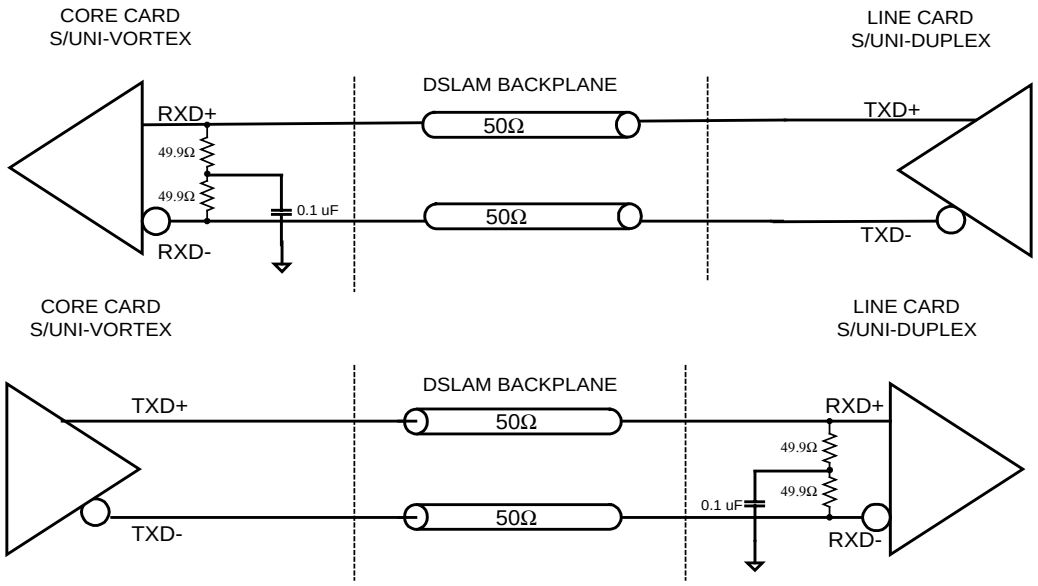
7.9 LVDS Design Notes

The low voltage differential signals should be routed together. The two traces that form a differential TX/RX path should have equal trace lengths from the chip to the connector. This is so any coupling on the TX/RX path is common-mode and not differential.

Traces for the LVDS signals should have controlled impedances. The two 49.9Ω differential receive termination resistors should be located as physically close to the chip as possible.

There are two methods of termination for the LVDS signals, selectable through onboard jumpers. The first method, depicted in Figure 5, is used for LVDS lines that interface to the DSLAM backplane.

Figure 5 - LVDS Backplane Termination Scheme



Backplane Termination

The second method, depicted in Figure 6, is used for LVDS lines that interface to the front panel. Two additional termination methods are possible for front panel LVDS signals:

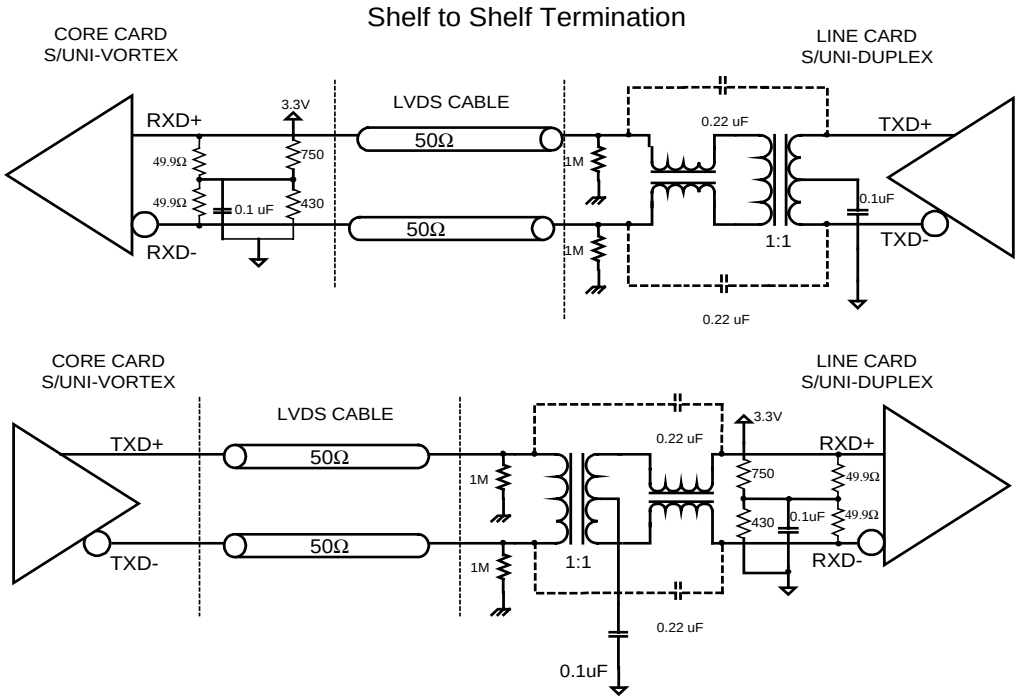
- Capacitive Coupling
- Transformer Coupling

Capacitive coupling, as indicated by the dashed lines offers a low cost, low board space alternative for LVDS signals that originate from shelves on the same ground system. To use the capacitive coupling option, do not install the transformers. Install the 0.22µF and 1MΩ resistors instead.

For shelf to shelf termination where the shelves are on different ground systems, transformers are required to provide isolation. Common mode chokes are also used to reduce the amount of radiated and received electromagnetic interference (EMI). Only one end of the connection requires transformers. These transformers are not used on the Core cord due to the large number of transformers that would be required to interface to both the Line and WAN Cards.

To use the transformer coupling option, do not install the 0.22 µF or 1MΩ resistors. Install the transformer instead.

Figure 6 - LVDS Front Panel Termination Scheme



In all termination methods, the LVDS receive signals are terminated by two 49.9Ω resistors and a 0.1uF capacitor. This termination network should be placed as physically close to the S/UNI-DUPLEX as possible.

8 BOARD MODIFICATIONS

The following board modifications were made to the DSLAM Line Card.

- The R/WB trace to the FPGA U61 was missing from the layout. A wire from U42 pin 24 to U61 pin 74 reconnects R/WB to the FPGA.
- The FPGA internal registers were not reset on power-up. A wire from U65 pin 8 to U61 pin 112 labeled FPGA4 connects RESETB to the FPGA.
- Hot Swappable long pins are not installed so early power is not available. Resistors R31 and R32, both 0 Ω, are not populated.
- After device characterization, filter circuits for the S/UNI-DUPLEX have been modified. Filter recommendations are:
    - QAVD: R225 changed from 1.0kΩ to 0Ω, C45, 22uF, is removed.
    - CAVD: R258 changed from 20Ω to 5Ω, C50 changed from 22uF to 1uF.
    - RAVD: R259 changed from 20Ω to 0Ω, C51, 22uF, is removed.
    - TAVD: R260 changed from 3.3Ω to 0Ω, C52, 22uF, is removed.

APPENDIX A: SCHEMATICS

This schematic contains 34 pages as follows:

Sheet 1: Root Drawing

This sheet provides a block view of the interface signals between each block of the DSLAM Line Card Reference Design.

Sheet 2 – 3: S/UNI-DUPLEX Blocks

These 2 sheets show the connections needed for the S/UNI-DUPLEX device. It also shows the interface for the LVDS connection.

Sheet 4: CPCI Interface

This sheet shows the cPCI connector J1 and the power supply circuit. It also contains the mechanical mounting and grounding needed for a cPCI board.

Sheet 5: LVDS Interface

This sheet contains the connector used to carry the LVDS signals across a backplane.

Sheet 6: Microprocessor Block

This sheet contains the Microprocessor and the signals used to interface the MC68340.

Sheet 7 – 8: Microprocessor Interface

These sheets show the devices necessary to complete an entire microprocessor interface including ROM, RAM and an FPGA for address decoding.

Sheet 9: Front Panel

This sheet shows the front panel connector for the 16 TIP/RING pairs used for the line interface to the COMET device.

Sheet 10 – 17: Line Interface Blocks

These 8 sheets contain the line interface to the COMET device.

Sheet 18 – 33: COMET Blocks

These 16 sheets show the connections for the COMET device.

Sheet 34: Loopback Test Jig

This sheet is not necessary as part of this design. It was used to create a test jig to interface to the Line Card.

REVISIONS				
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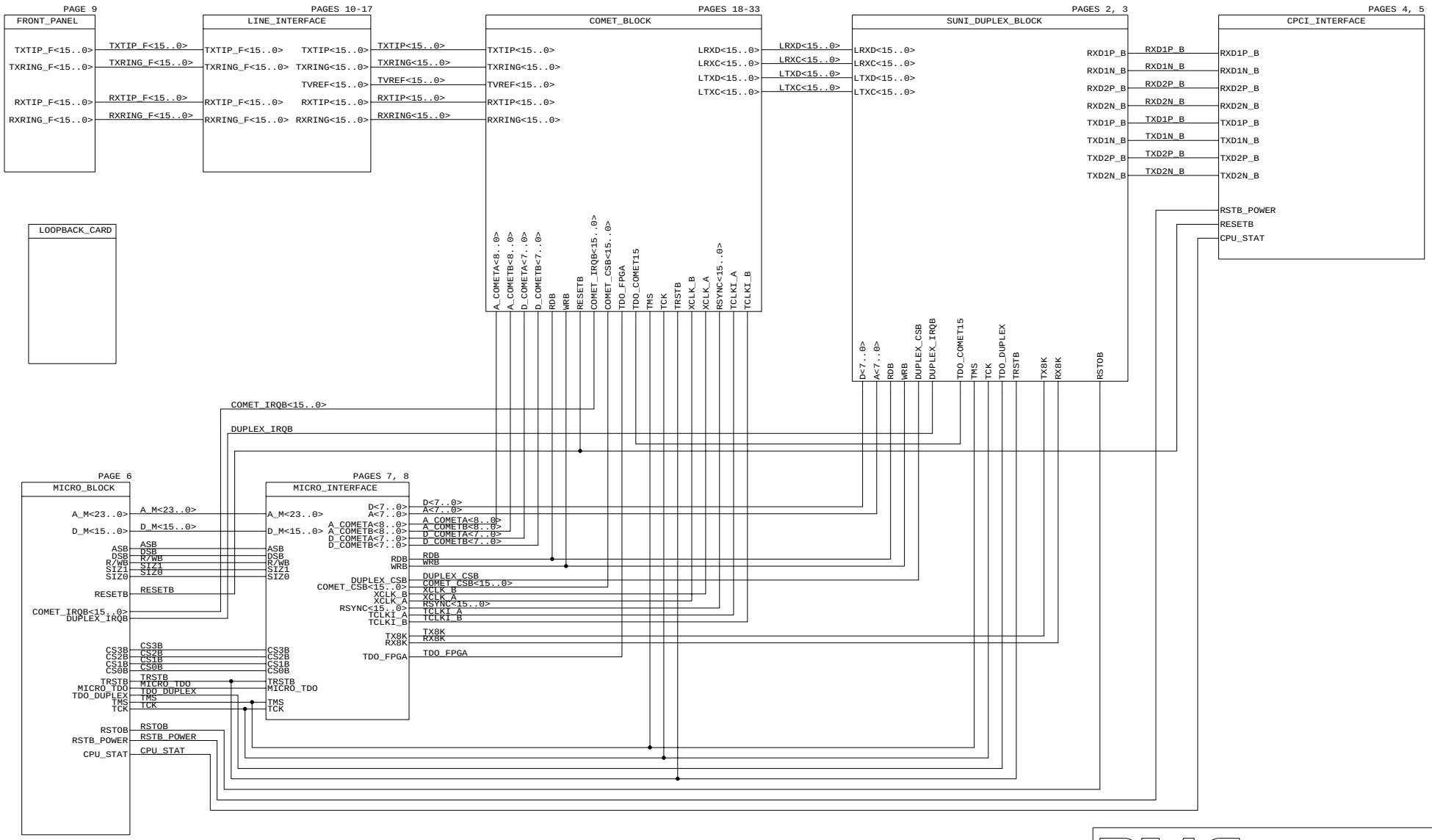

NOTE: ALL TRACES ARE 75 OHMS UNLESS OTHERWISE NOTED

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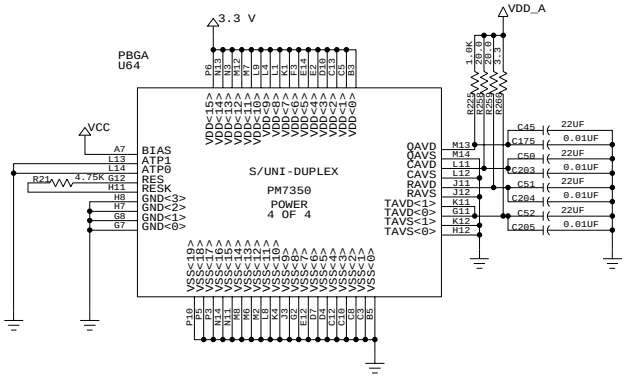
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD ROOT DRAWING	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:1 OF 33

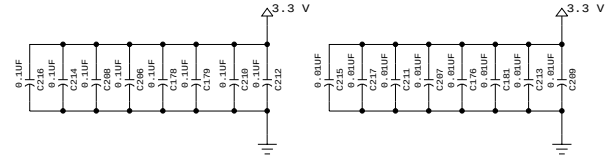
NOTE: VCC = +5V
NOTE: VDD_A = +3.3V

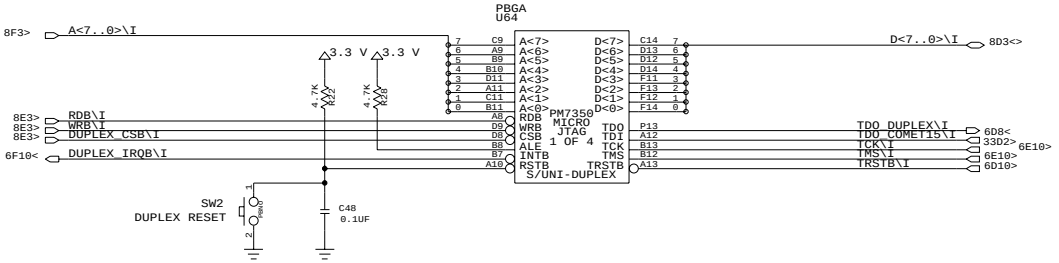
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

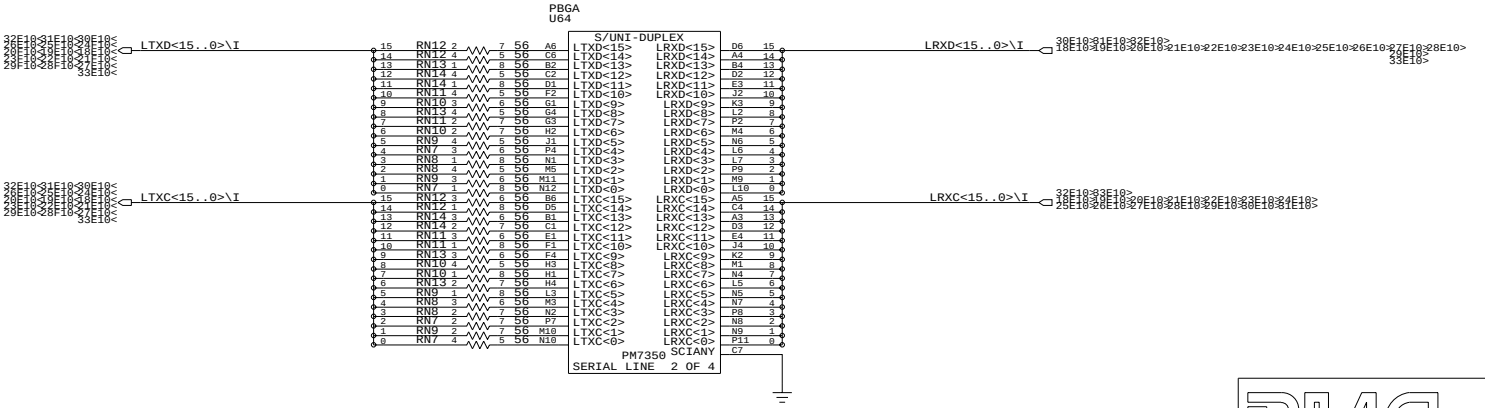
NOTE: PLACE FILTER NETWORKS AS PHYSICALLY CLOSE TO THE DEVICE AS POSSIBLE.



ALTERNATE CAPS ON SUNI-DUPLEX VDD PINS







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PMC-Sierra, Inc.

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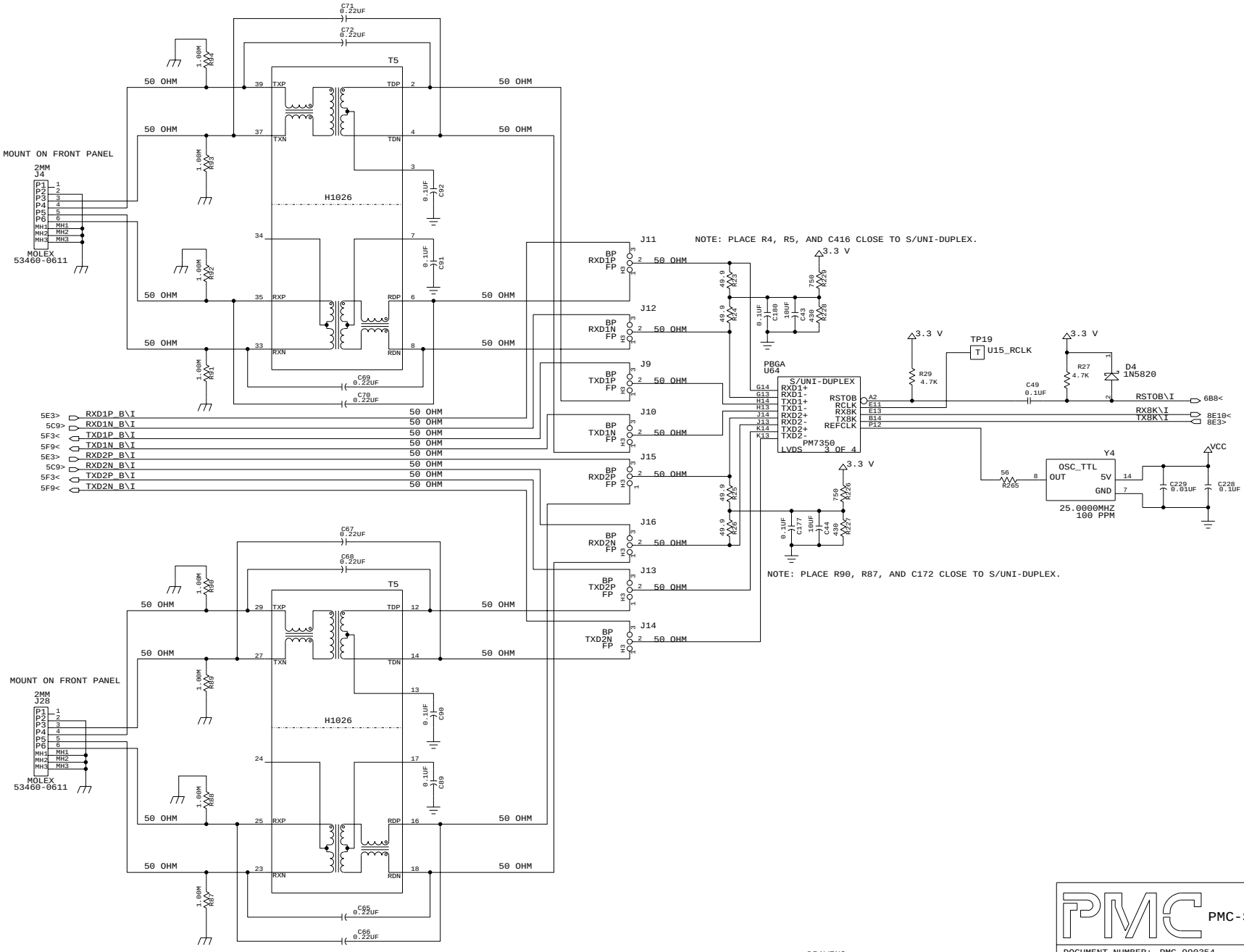
TITLE: DSLAM LINE CARD S/UNI-DUPLEX BLOCK 1	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:2 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE: VCC = +5V

NOTE: INSTALL EITHER TRANSFORMER T5 OR CAPACITORS C408-C415 AND RESISTORS R237-R244



NOTE: PLACE R4, R5, AND C416 CLOSE TO S/UNI-DUPLEX.

NOTE: PLACE R90, R87, AND C172 CLOSE TO S/UNI-DUPLEX.

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:3 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

NOTE: VCC = +5V

INSTALL EITHER R126 (IF AVAILABLE),
OR R114-R119, R122-R125.

MOUNT LED ON FRONT PANEL

NOTE: VDD_A = 3.3V ANALOG

PLACE CORRECT SIZE MOUNTING HOLE

NOTE: TERMINAL BLOCK USED TO SUPPLY
POWER IF NO CPCI CONNECTOR EXISTS

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:4 OF 33

NOTE: VCC = +5V

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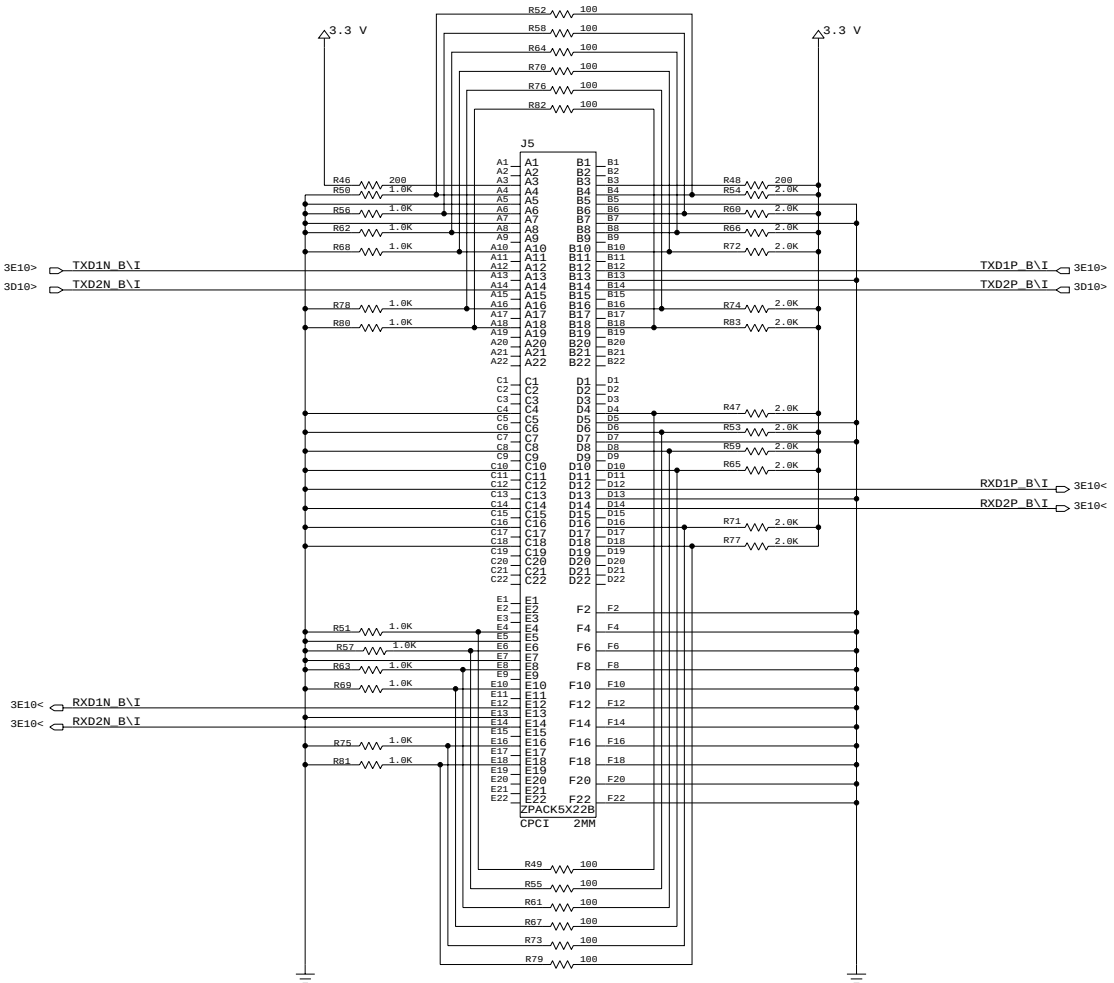

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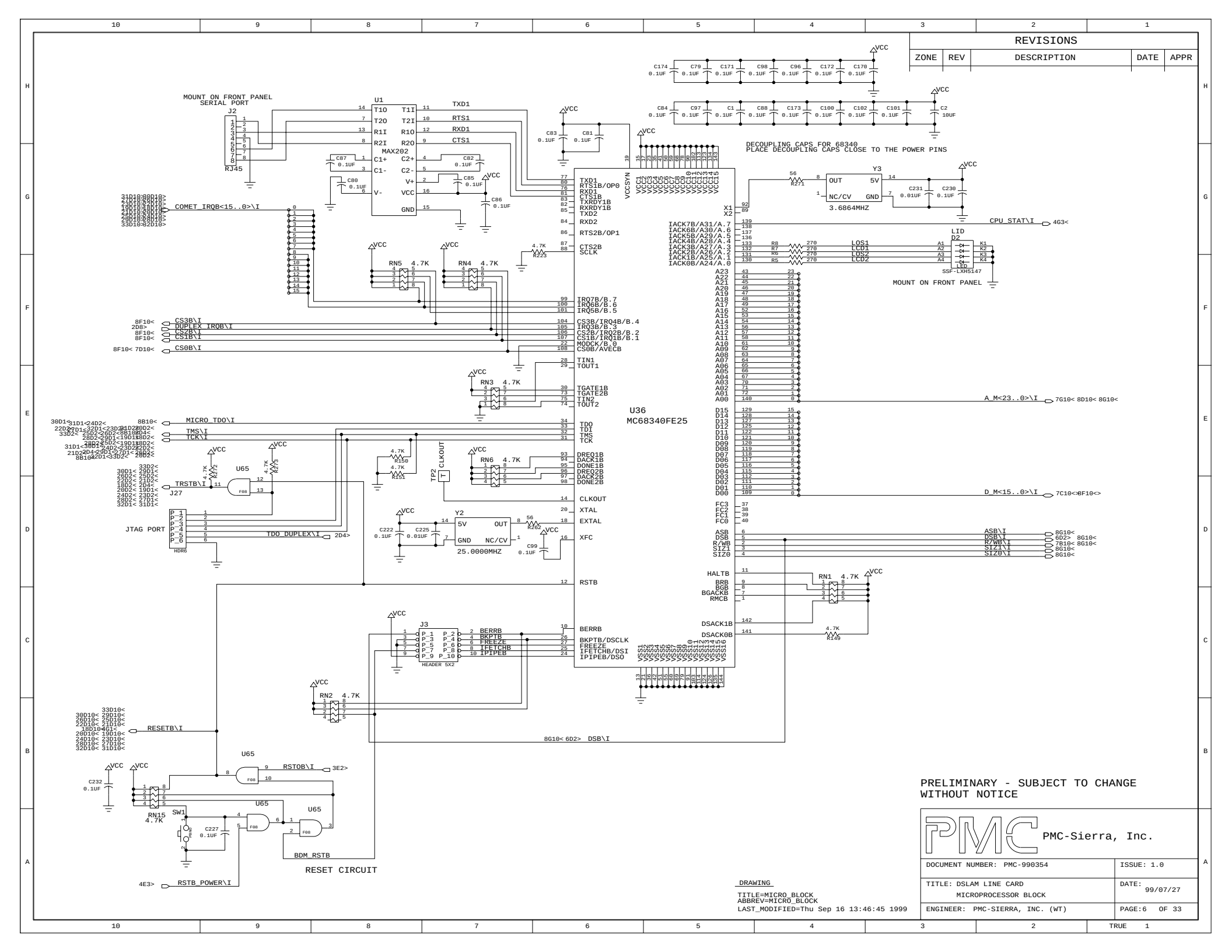
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:5 OF 33


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
MOUNT ON FRONT PANEL SERIAL PORT
J2
RJ45
U1
MAX202
TXD1
RTS1
RXD1
CTS1
DECOUPLING CAPS FOR 68340
PLACE DECOUPLING CAPS CLOSE TO THE POWER PINS
Y3
3.6864MHZ
CPU_STAT\I
LID
D2
SSF-LXH5147
MOUNT ON FRONT PANEL
COMET_IRQB<15..0>\I
RN5 4.7K
RN4 4.7K
RN3 4.7K
RN6 4.7K
RN1 4.7K
RN2 4.7K
CS3B\I
DUPLEX_IRQB\I
CS2B\I
CS1B\I
CS0B\I
U36
MC68340FE25
A_M<23..0>\I
D_M<15..0>\I
MICRO_TDO\I
TMS\I
TCK\I
TRSTB\I
J27
JTAG PORT
TDO_DUPLEX\I
CLKOUT
Y2
25.0000MHZ
J3
HEADER 5X2
RESETB\I
RSTOB\I
RSTB_POWER\I
BDM_RSTB
RESET CIRCUIT
DSB\I
PRELIMINARY - SUBJECT TO CHANGE
WITHOUT NOTICE
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-990354
ISSUE: 1.0
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MICROPROCESSOR BLOCK
DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)
PAGE:6 OF 33
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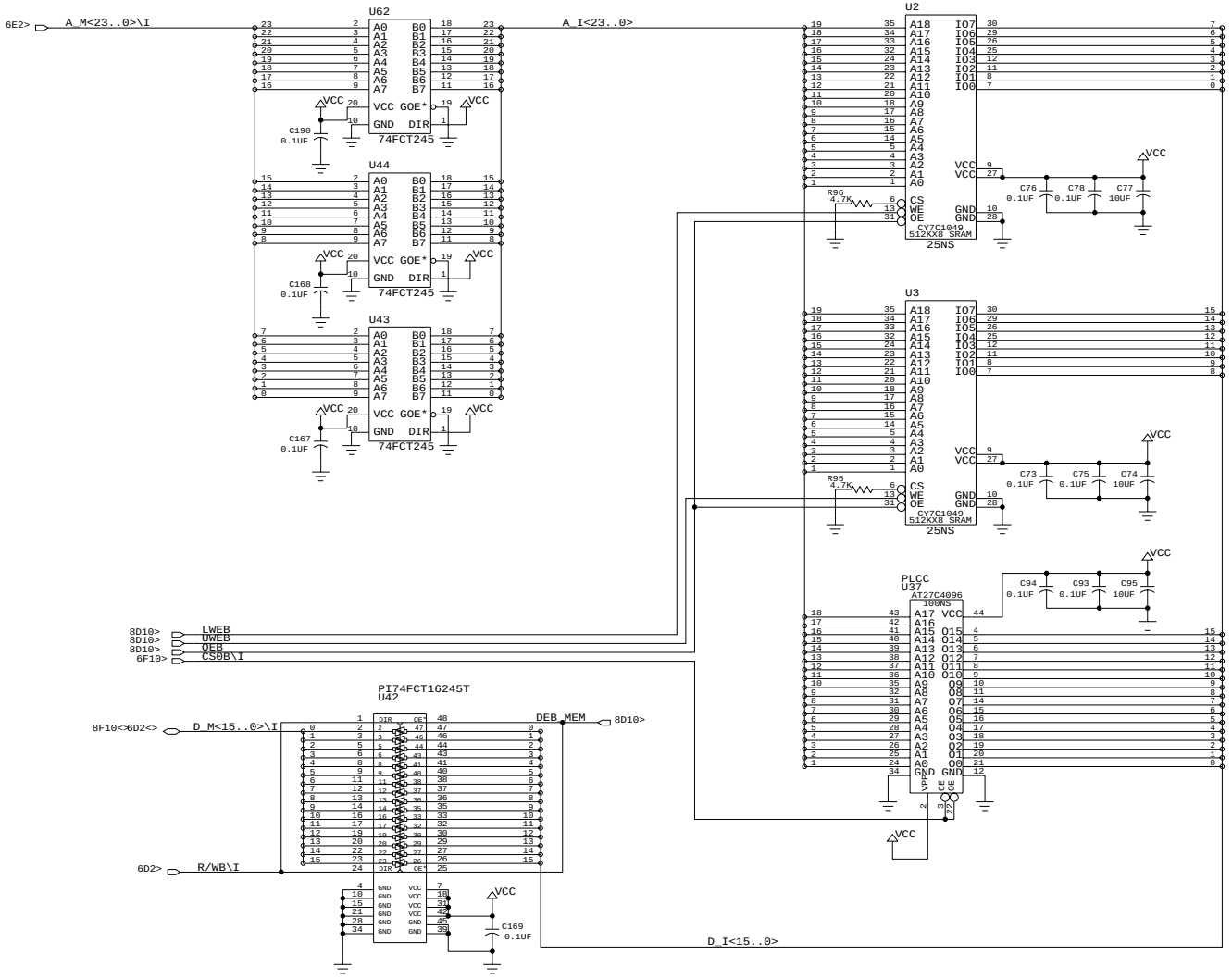

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:7 OF 33

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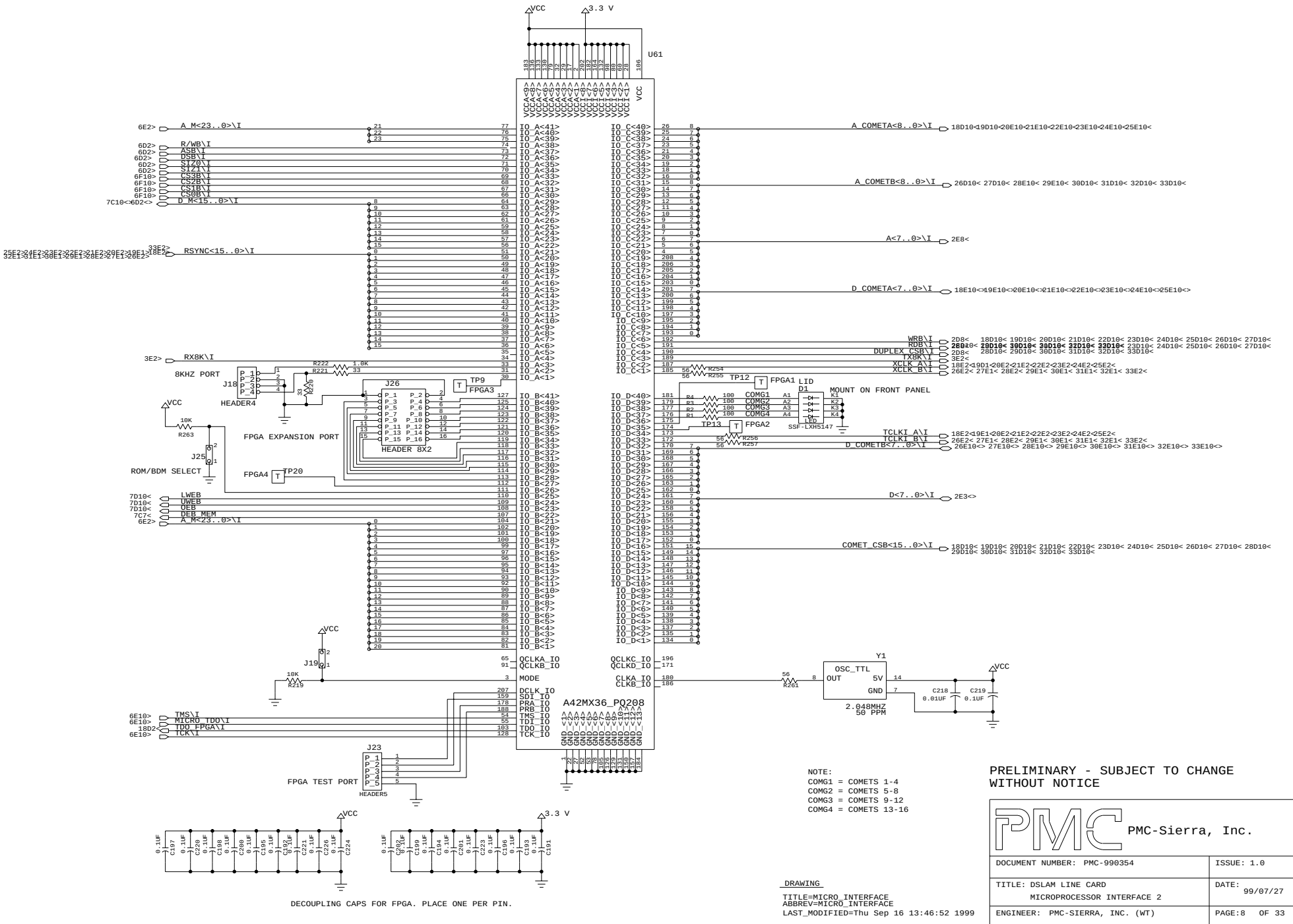

NOTE:
COMG1 = COMETS 1-4
COMG2 = COMETS 5-8
COMG3 = COMETS 9-12
COMG4 = COMETS 13-16

PRELIMINARY - SUBJECT TO CHANGE WITHOUT NOTICE

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PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:8 OF 33

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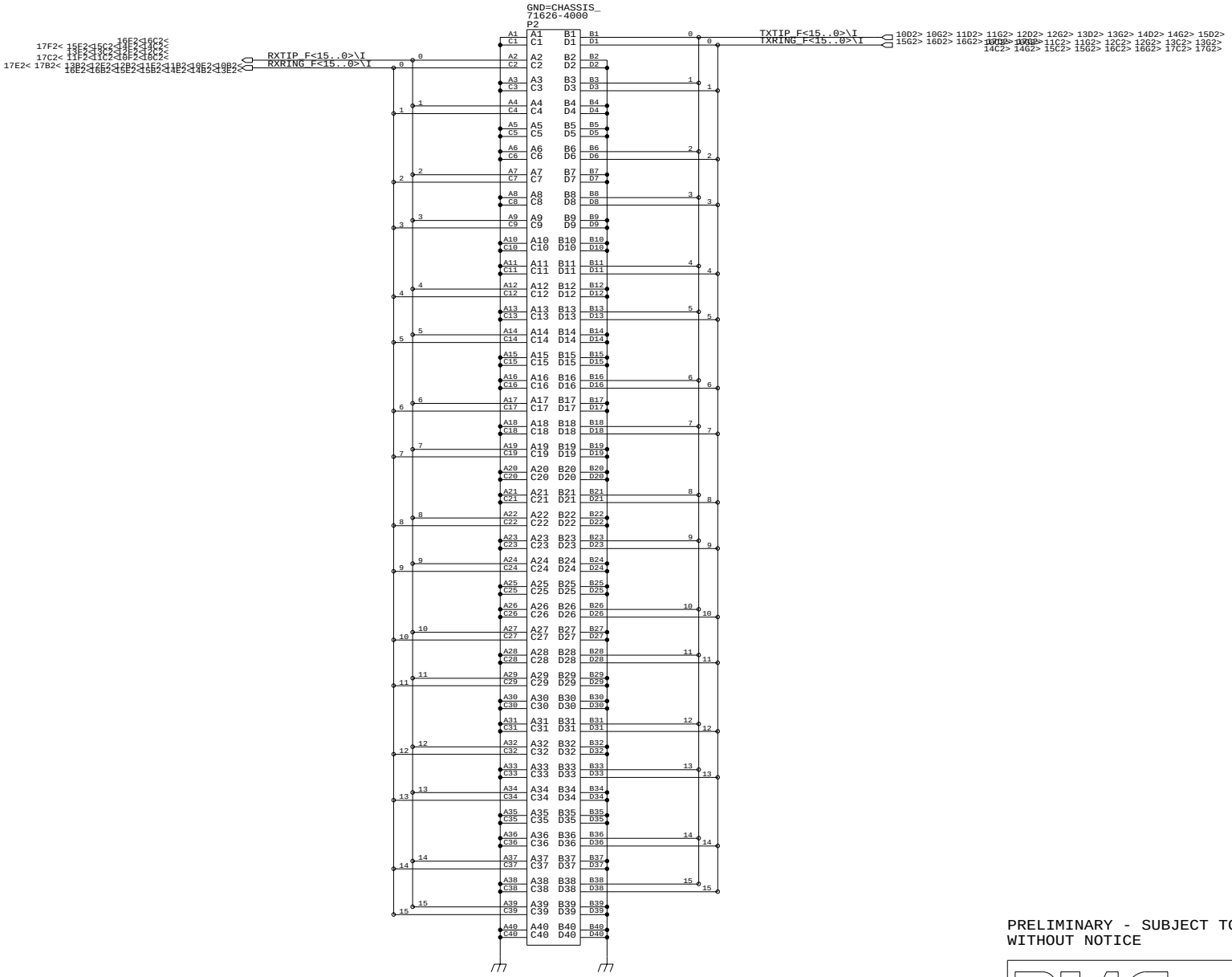

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:9 OF 33

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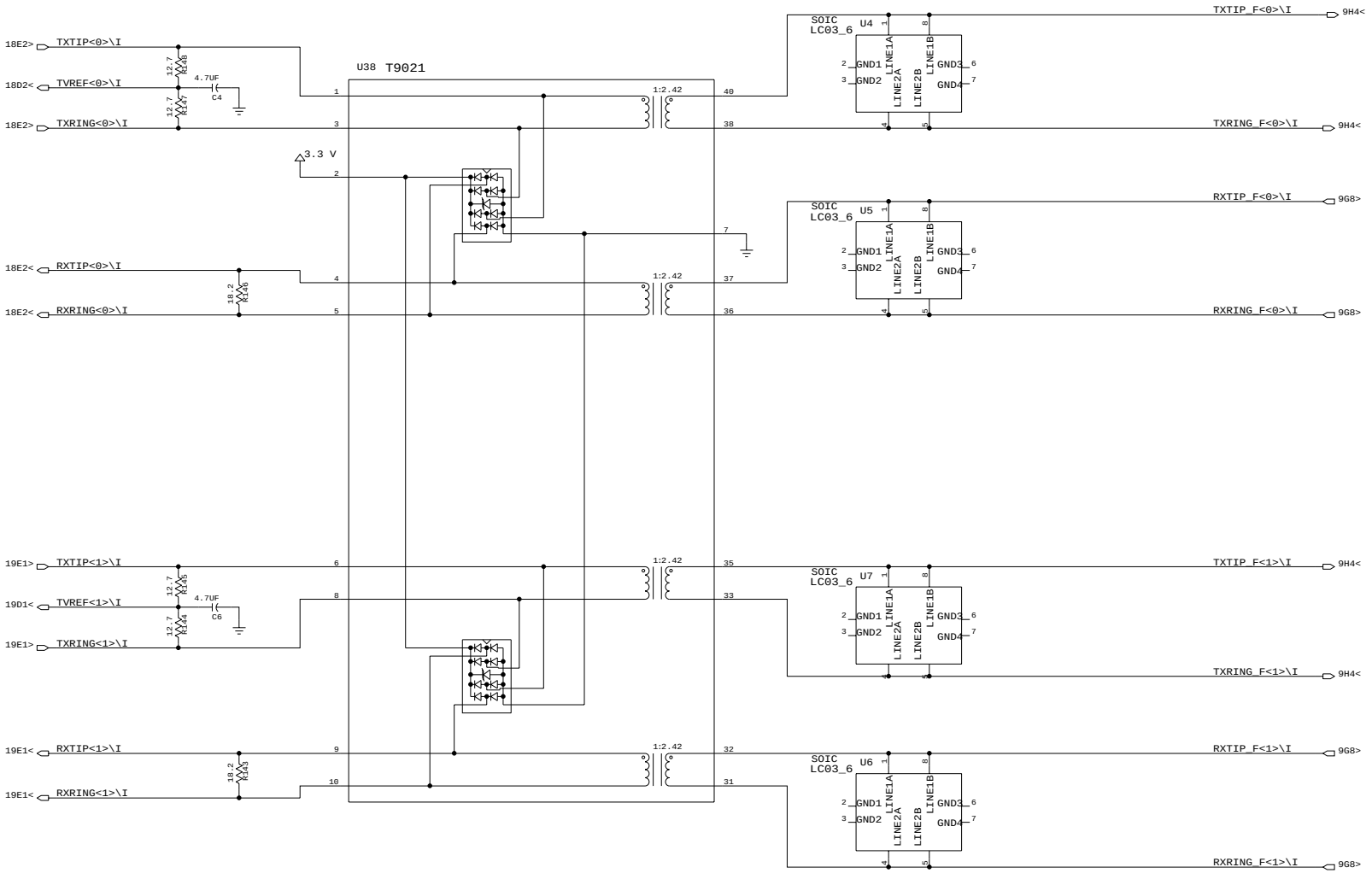

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:10 OF 33

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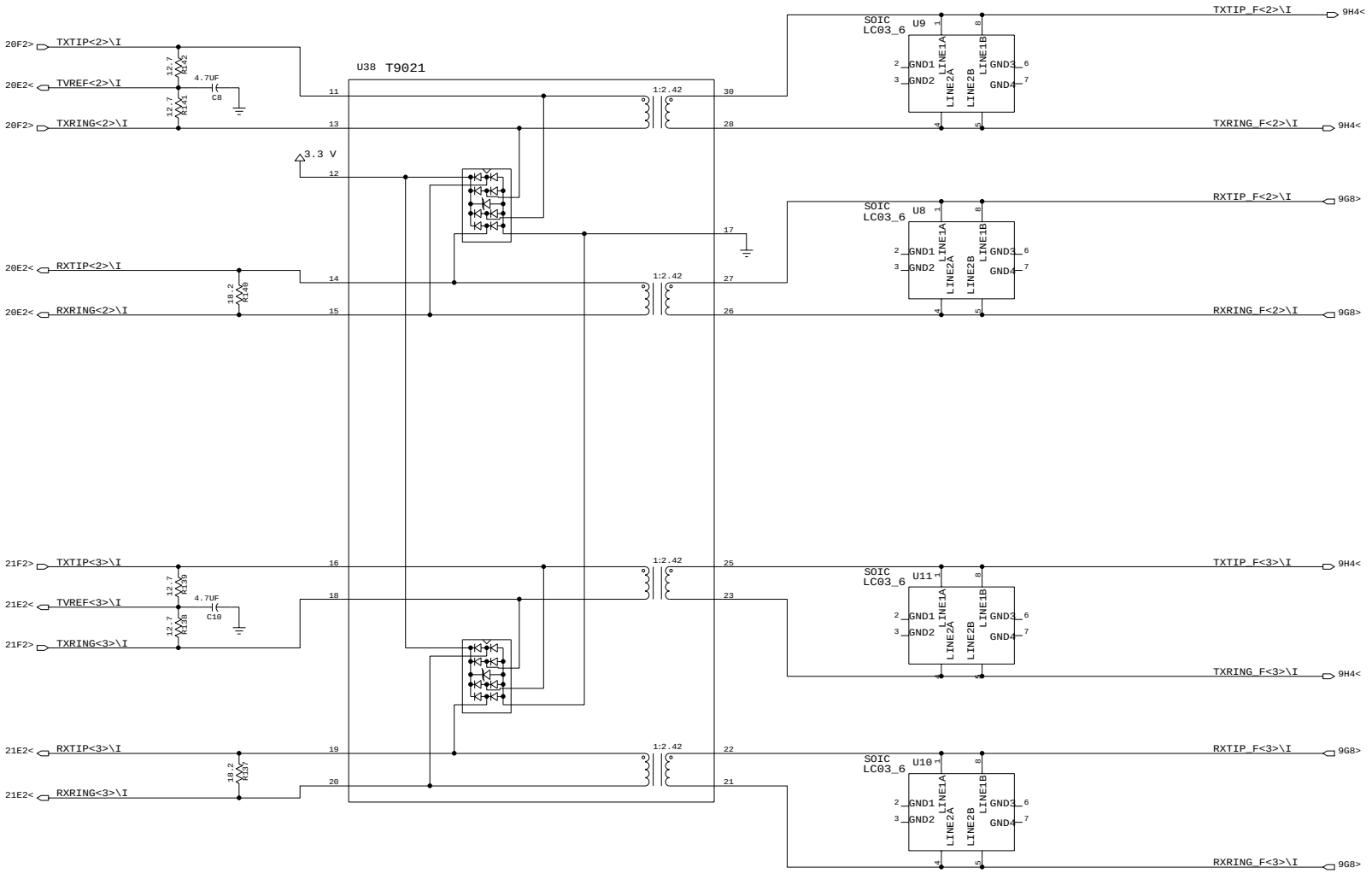

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:11 OF 33

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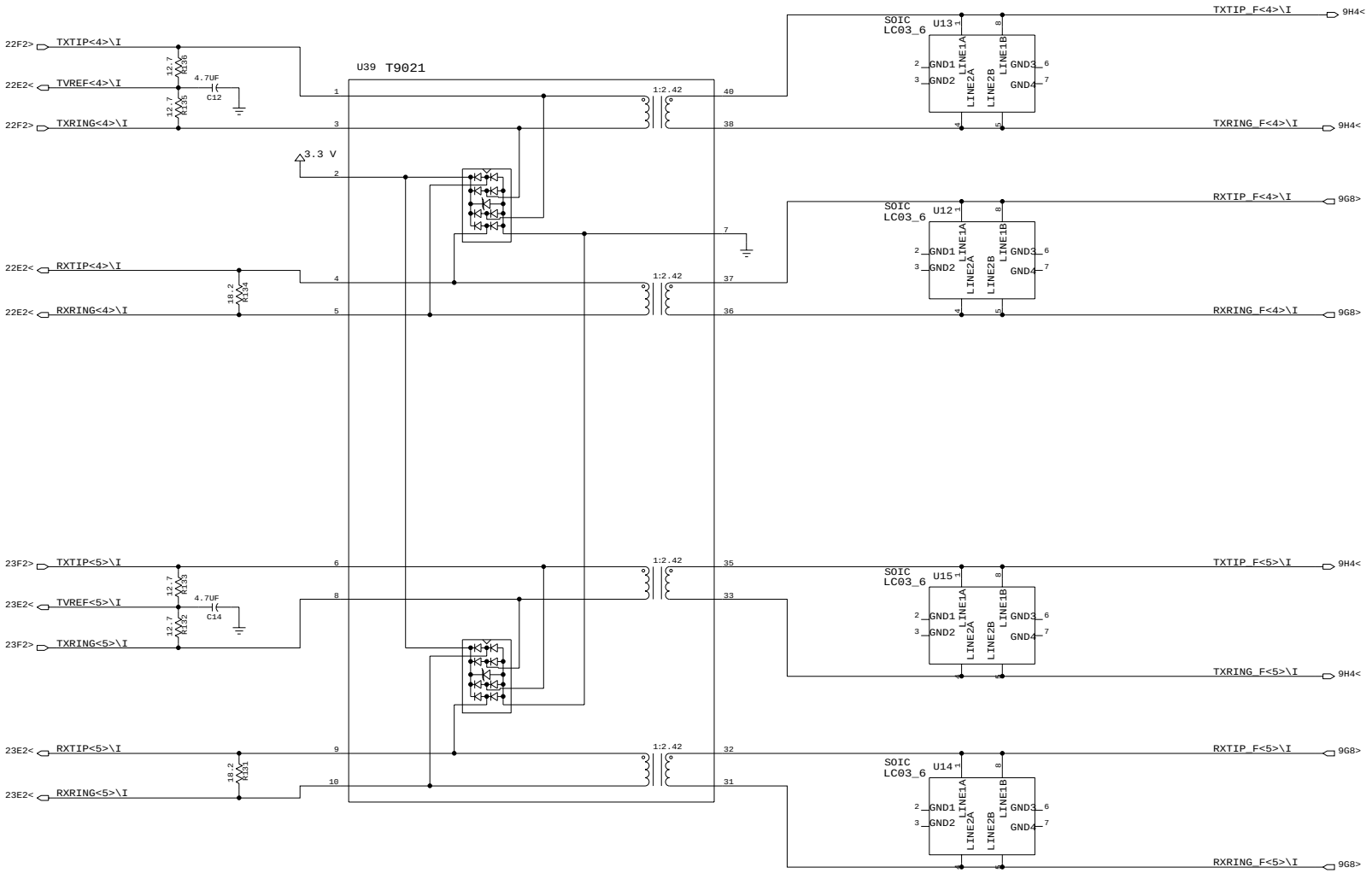

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:12 OF 33

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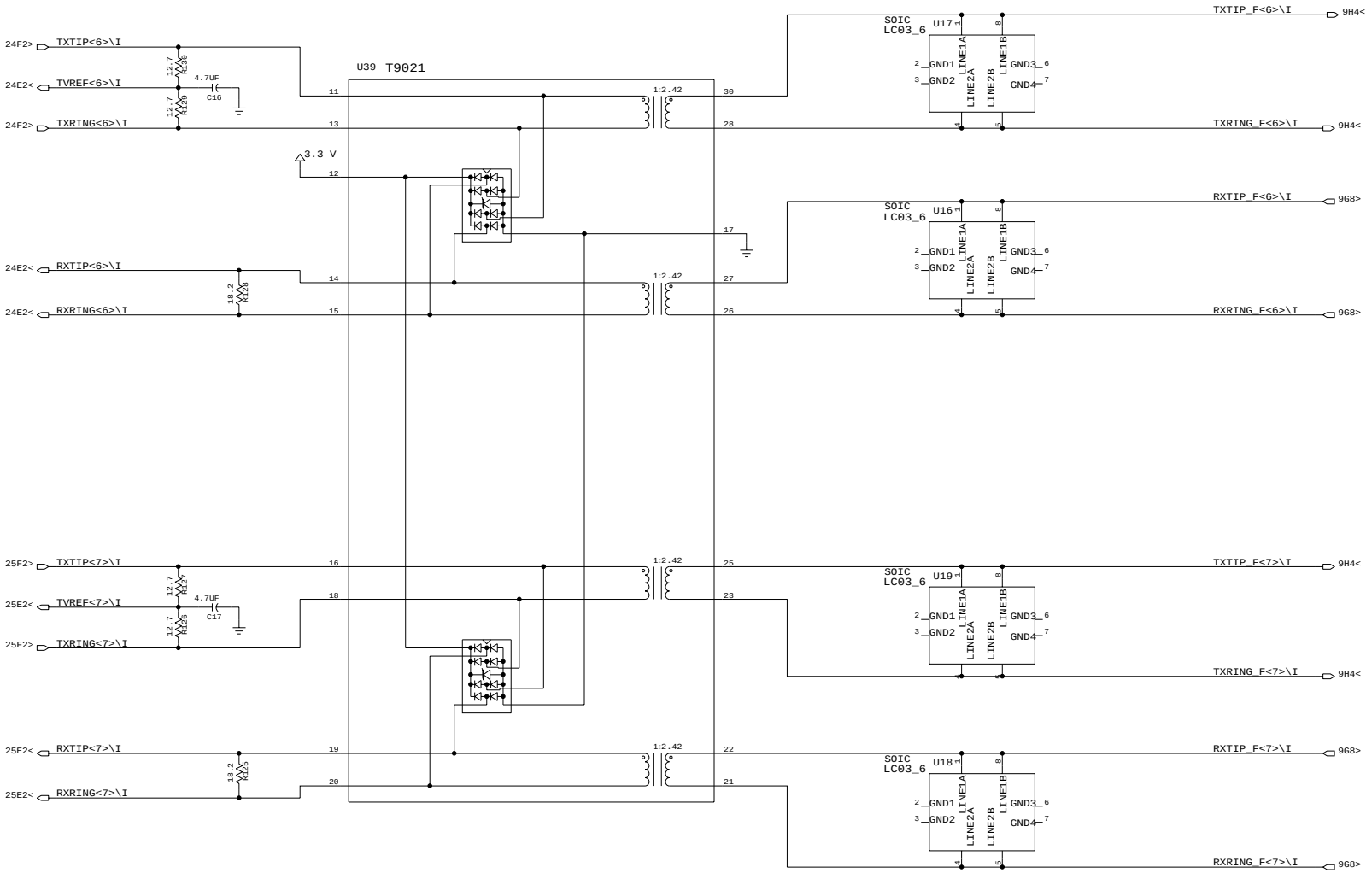

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:13 OF 33

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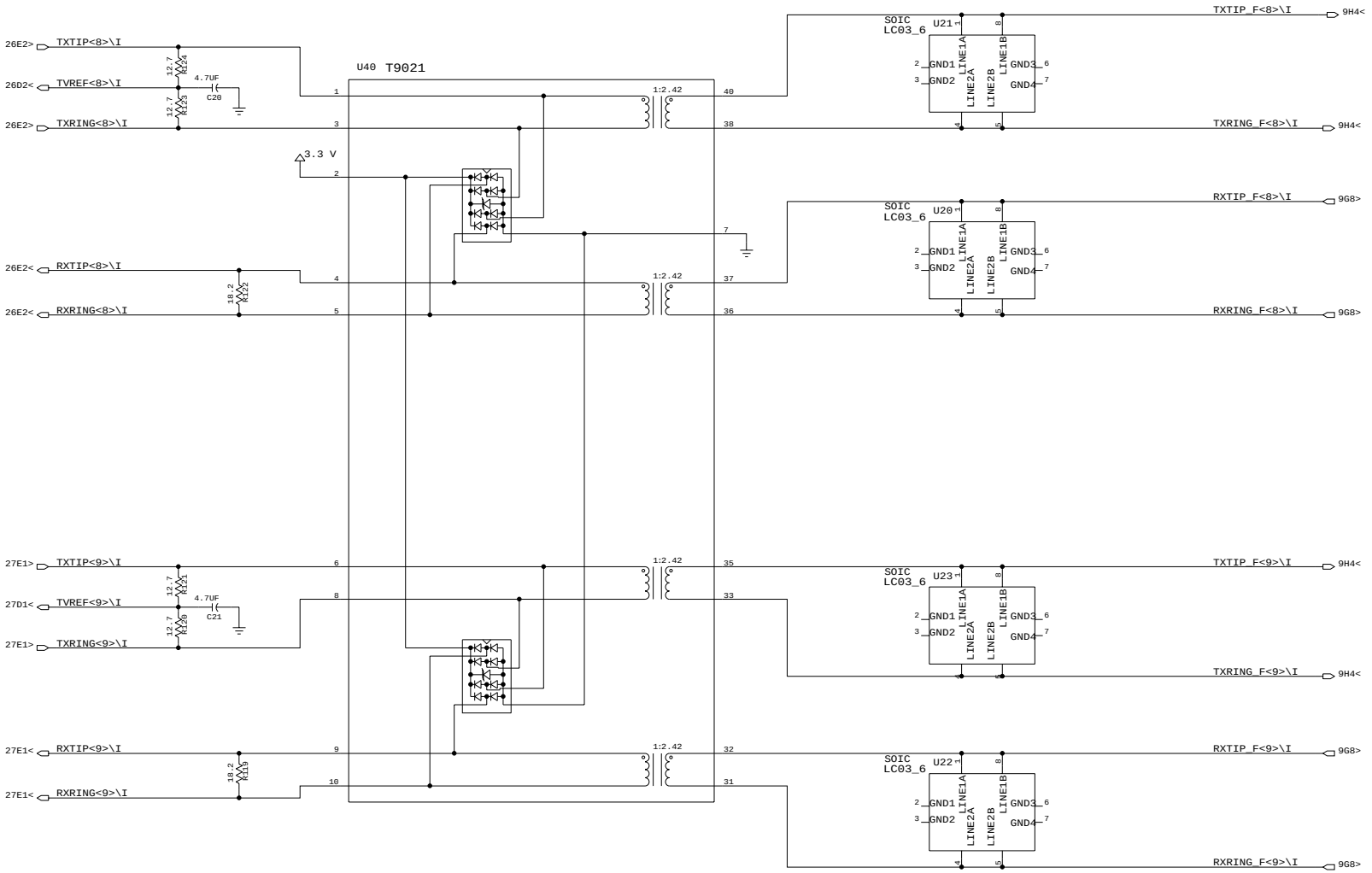

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:14 OF 33

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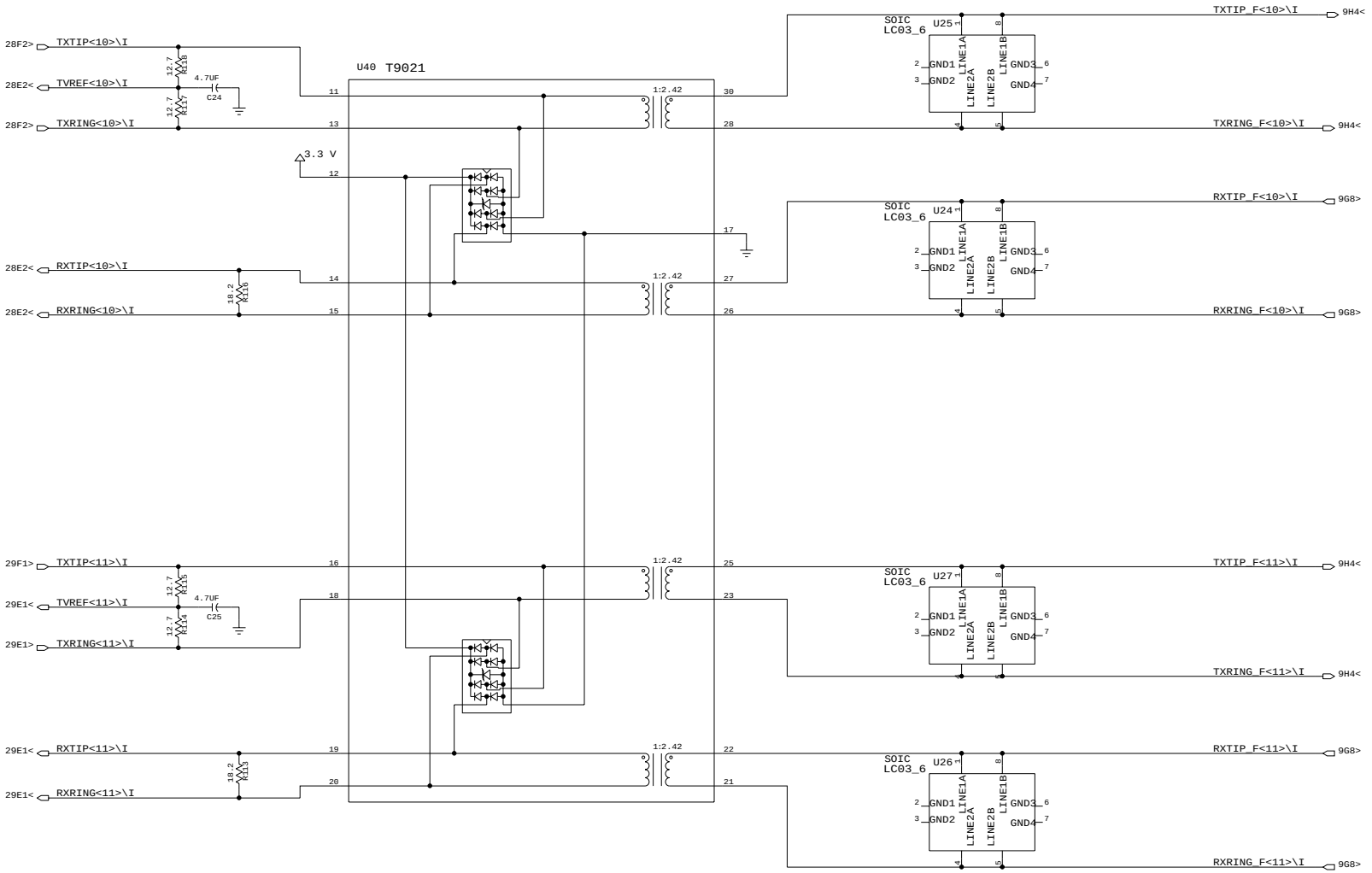

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:15 OF 33

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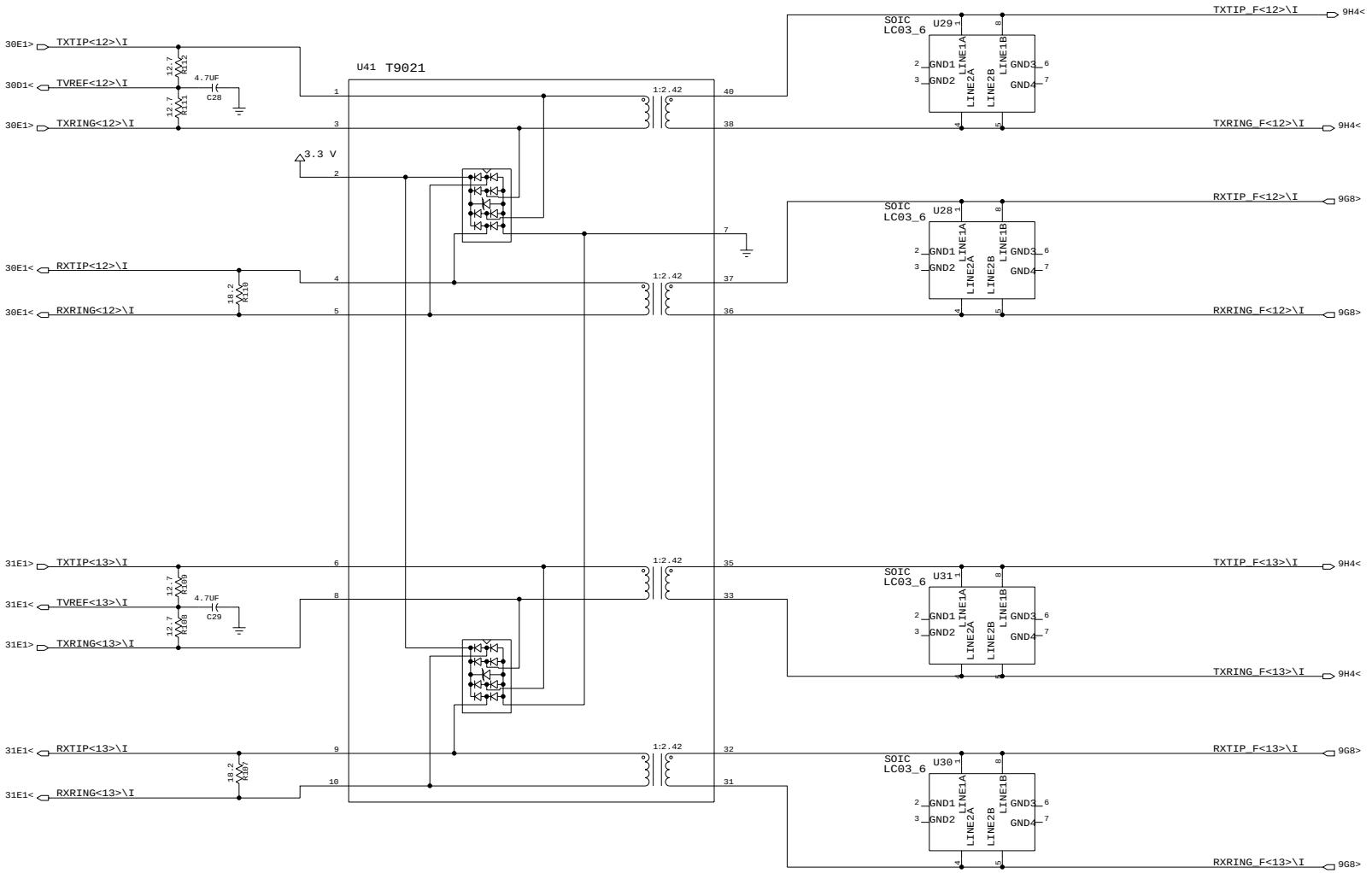

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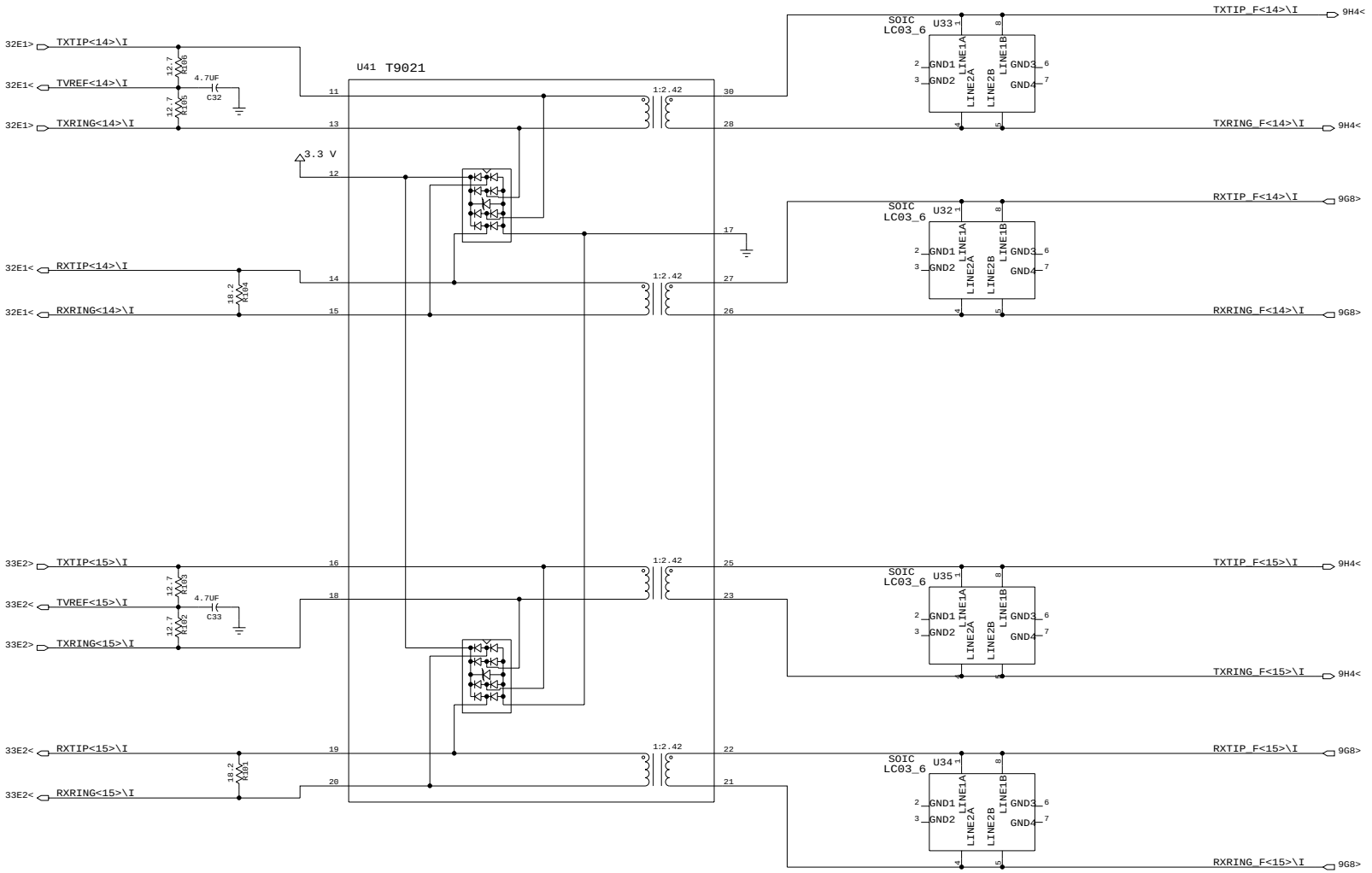

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:17 OF 33

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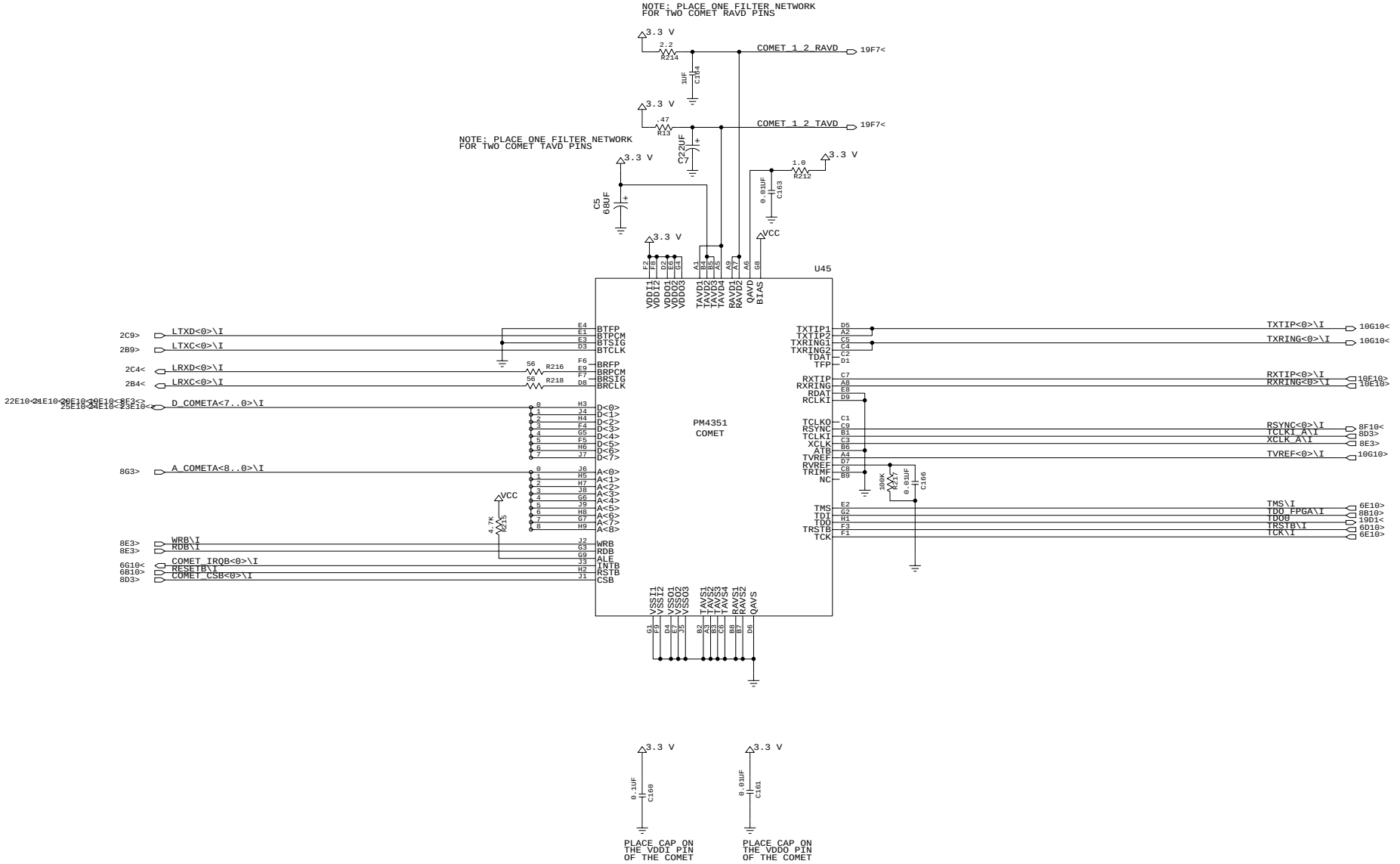

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:18 OF 33

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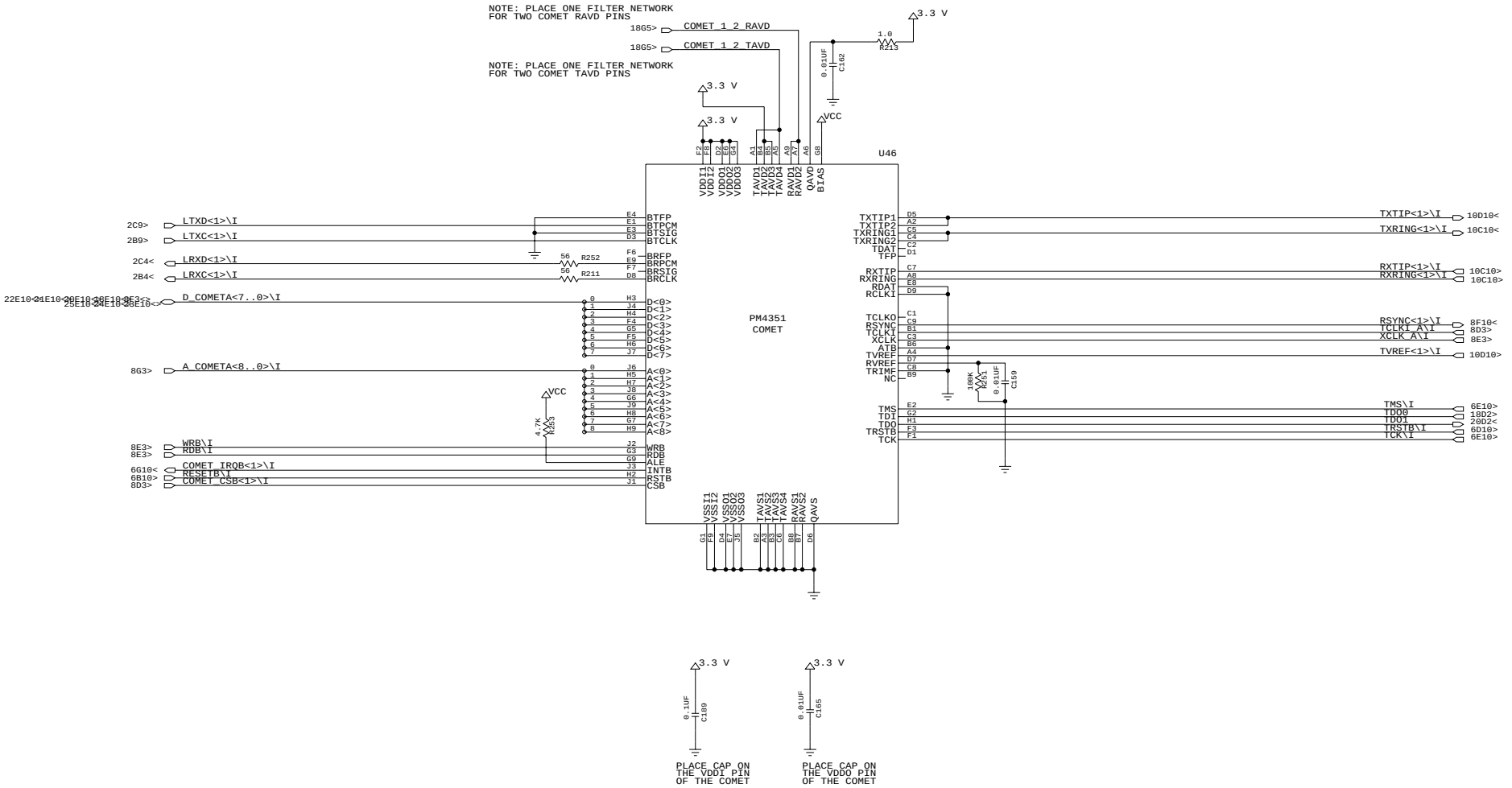

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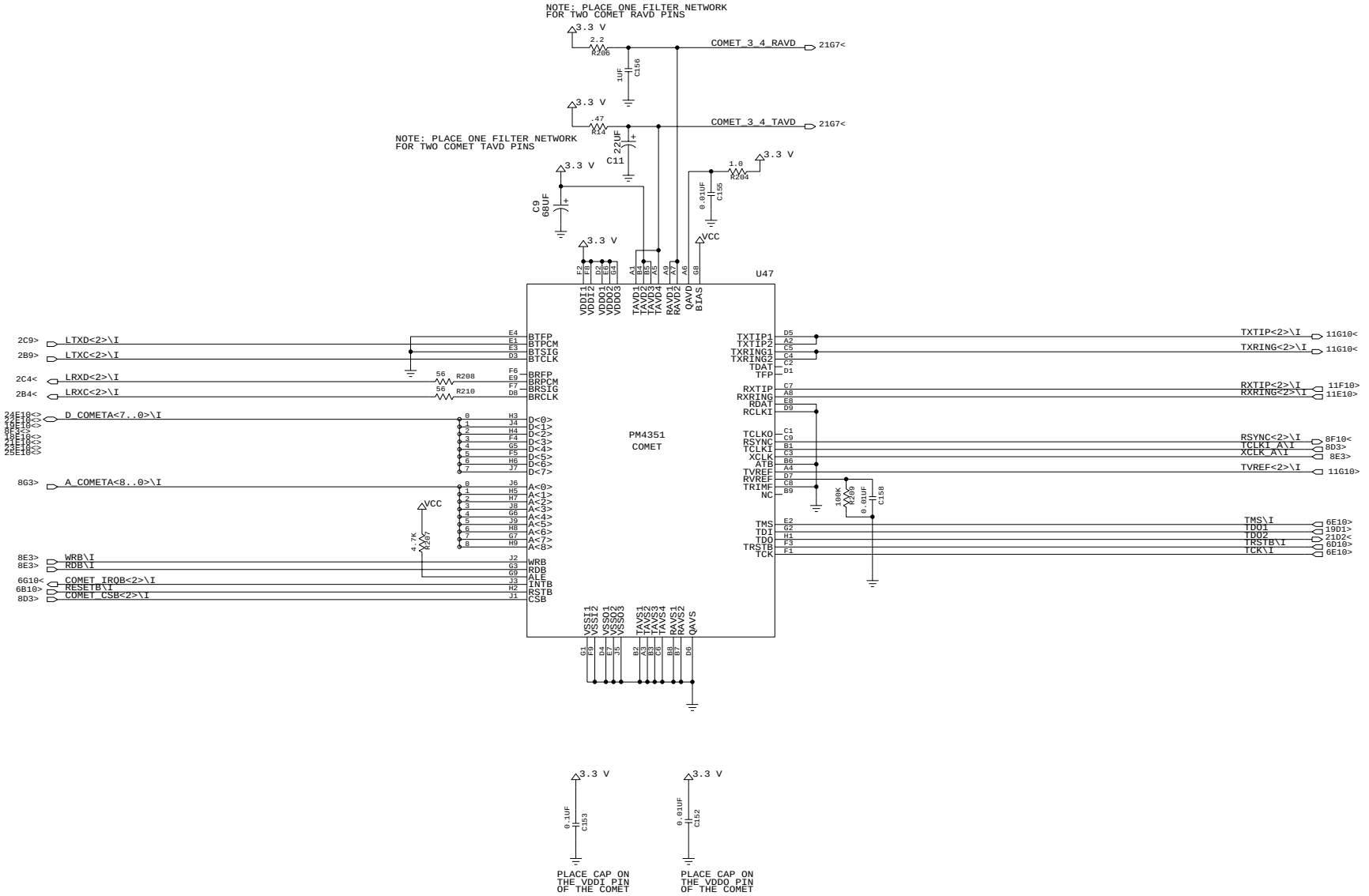

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ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:20 OF 33

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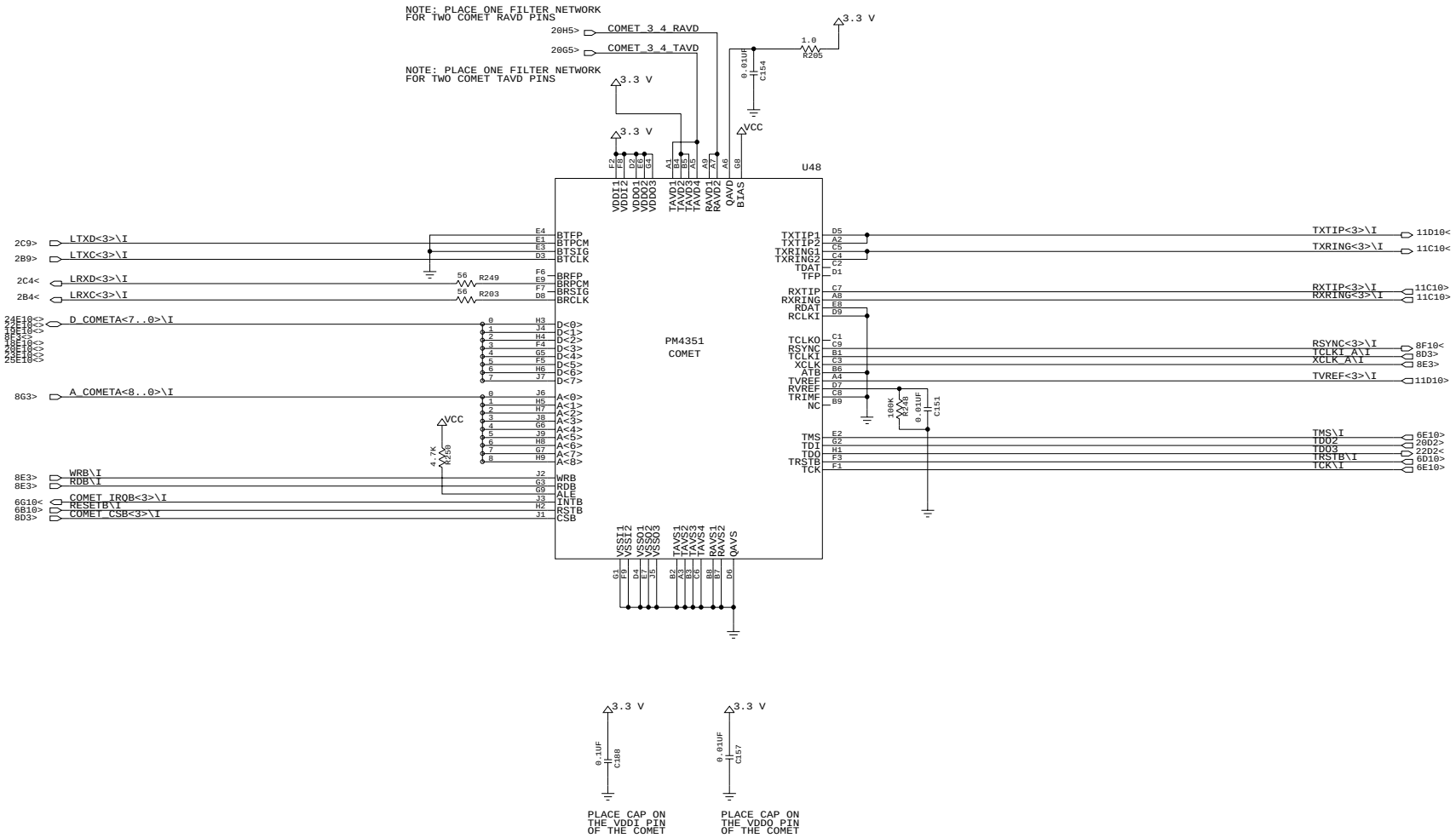

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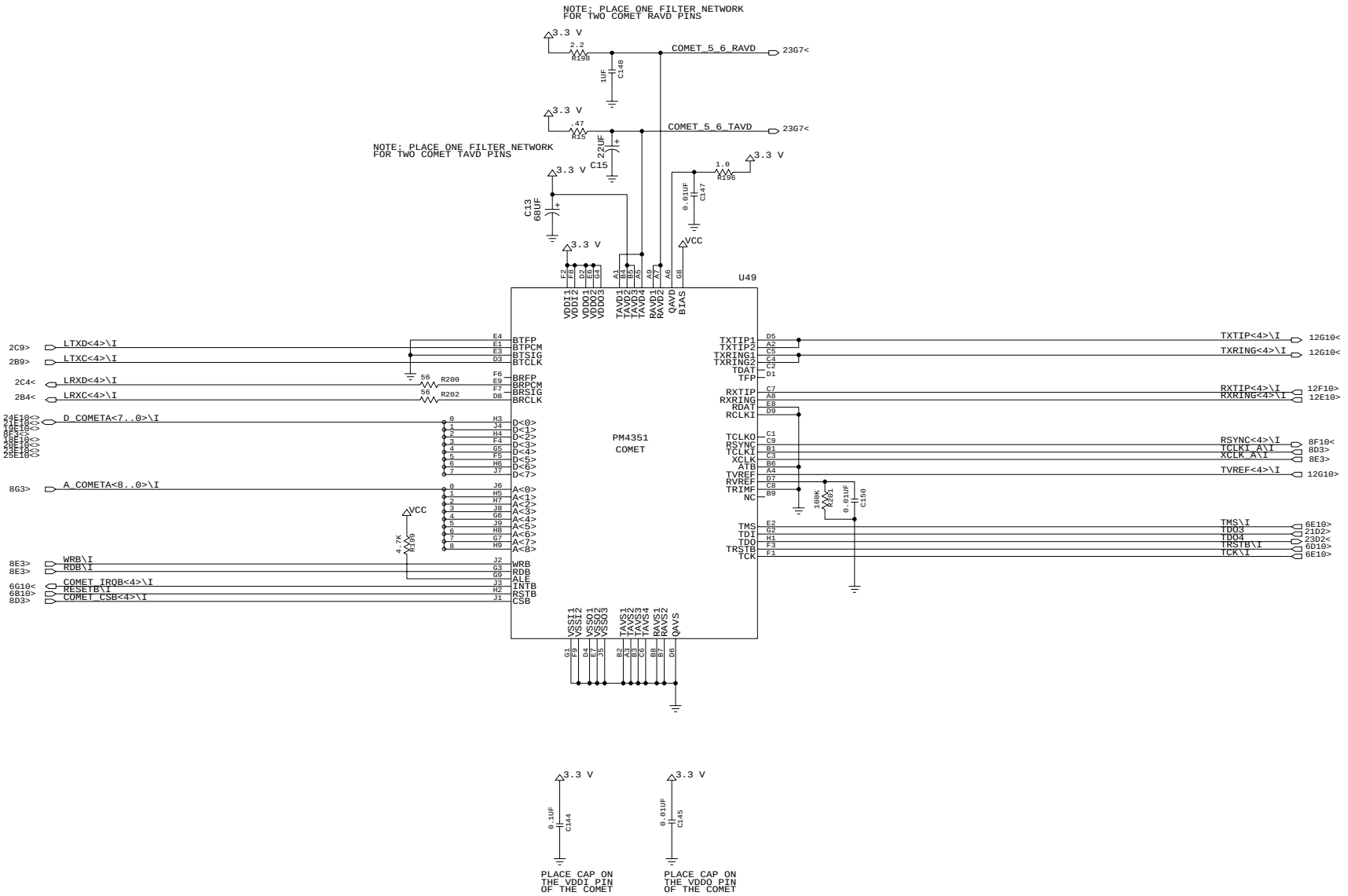
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:21 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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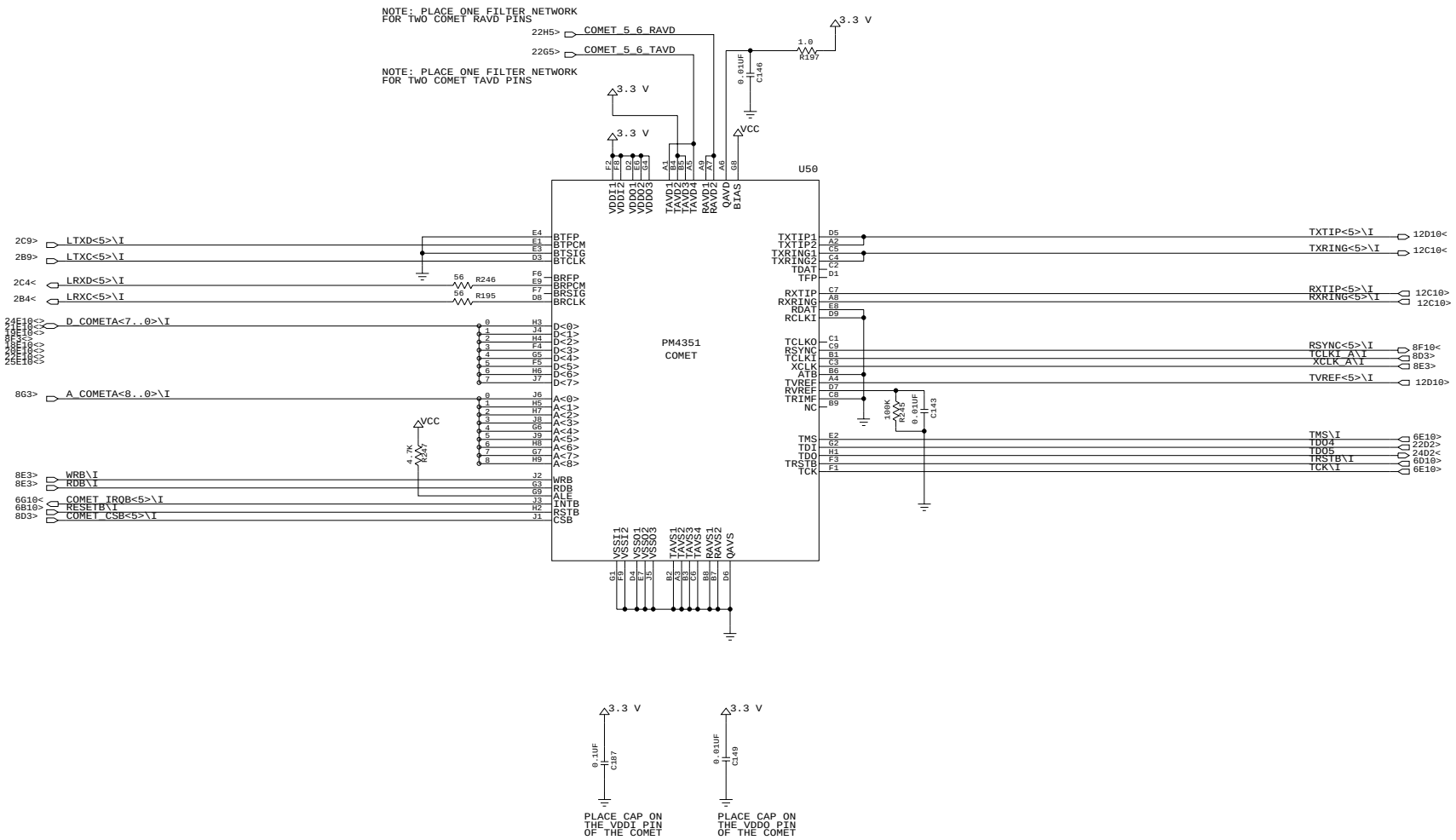
ABBREV=COMET_BLOCK
LAST_MODIFIED=Thu Sep 16 13:46:27 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 5	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:22 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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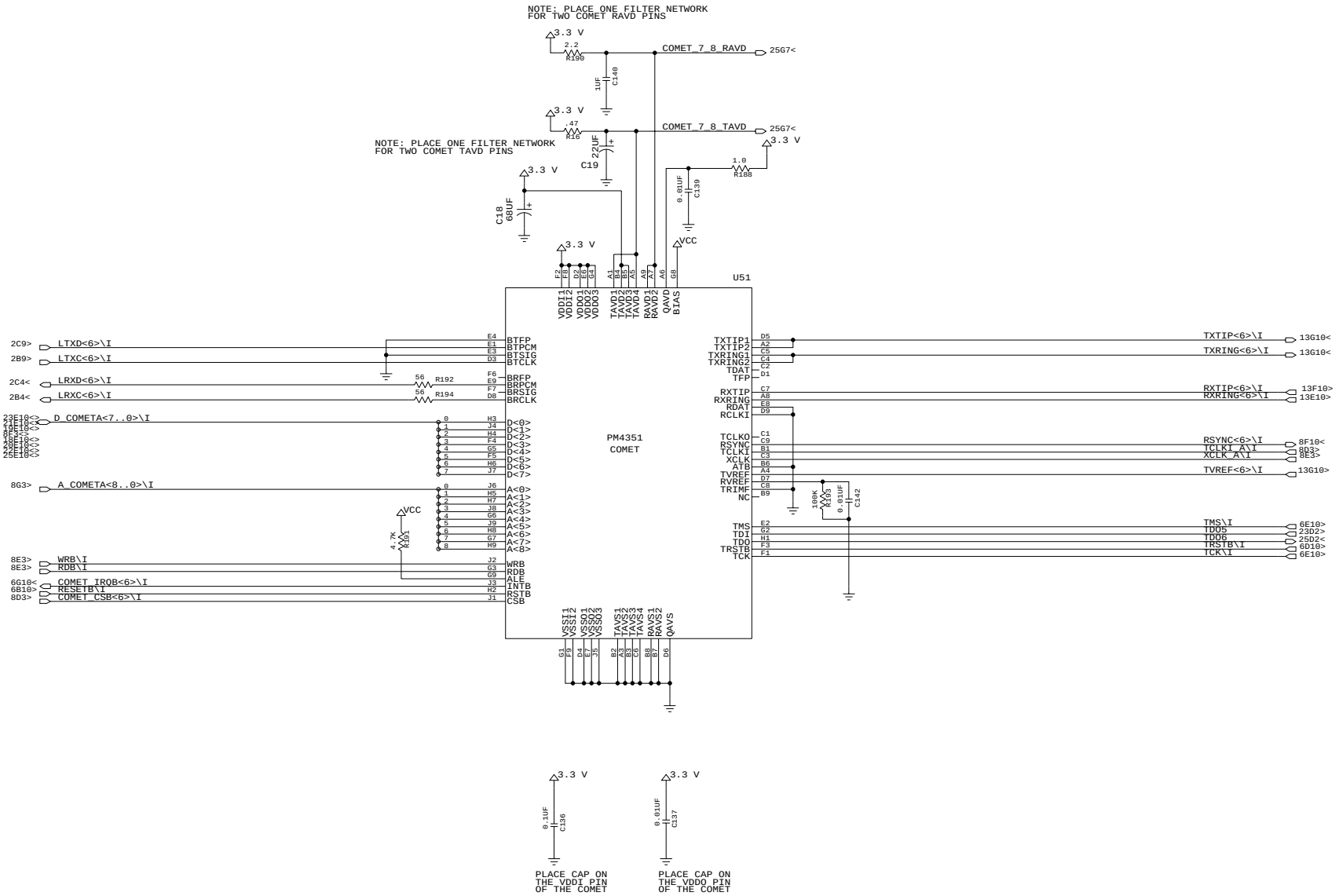
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 6	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:23 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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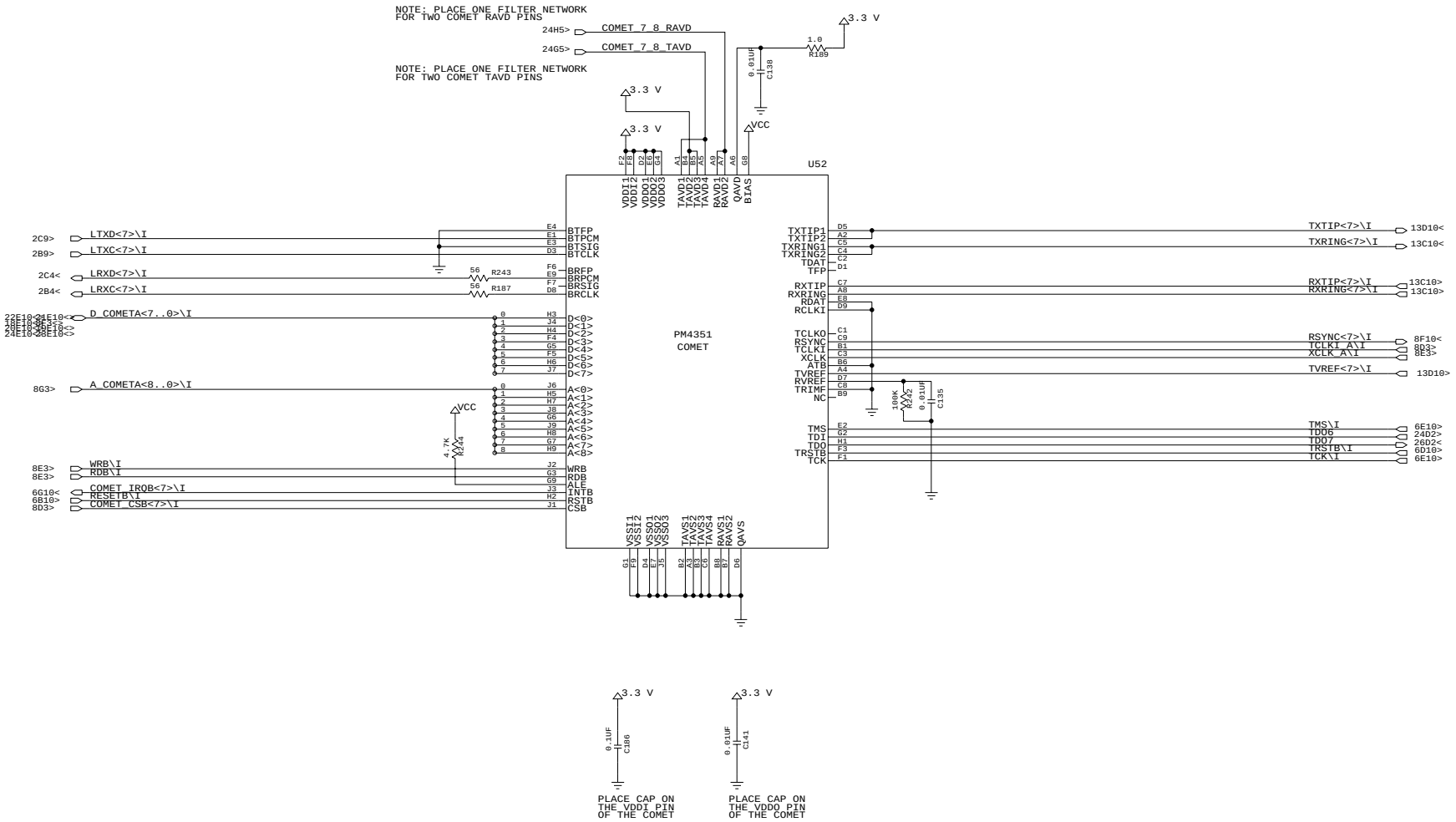
LAST_MODIFIED=Thu Sep 16 13:46:30 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 7	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:24 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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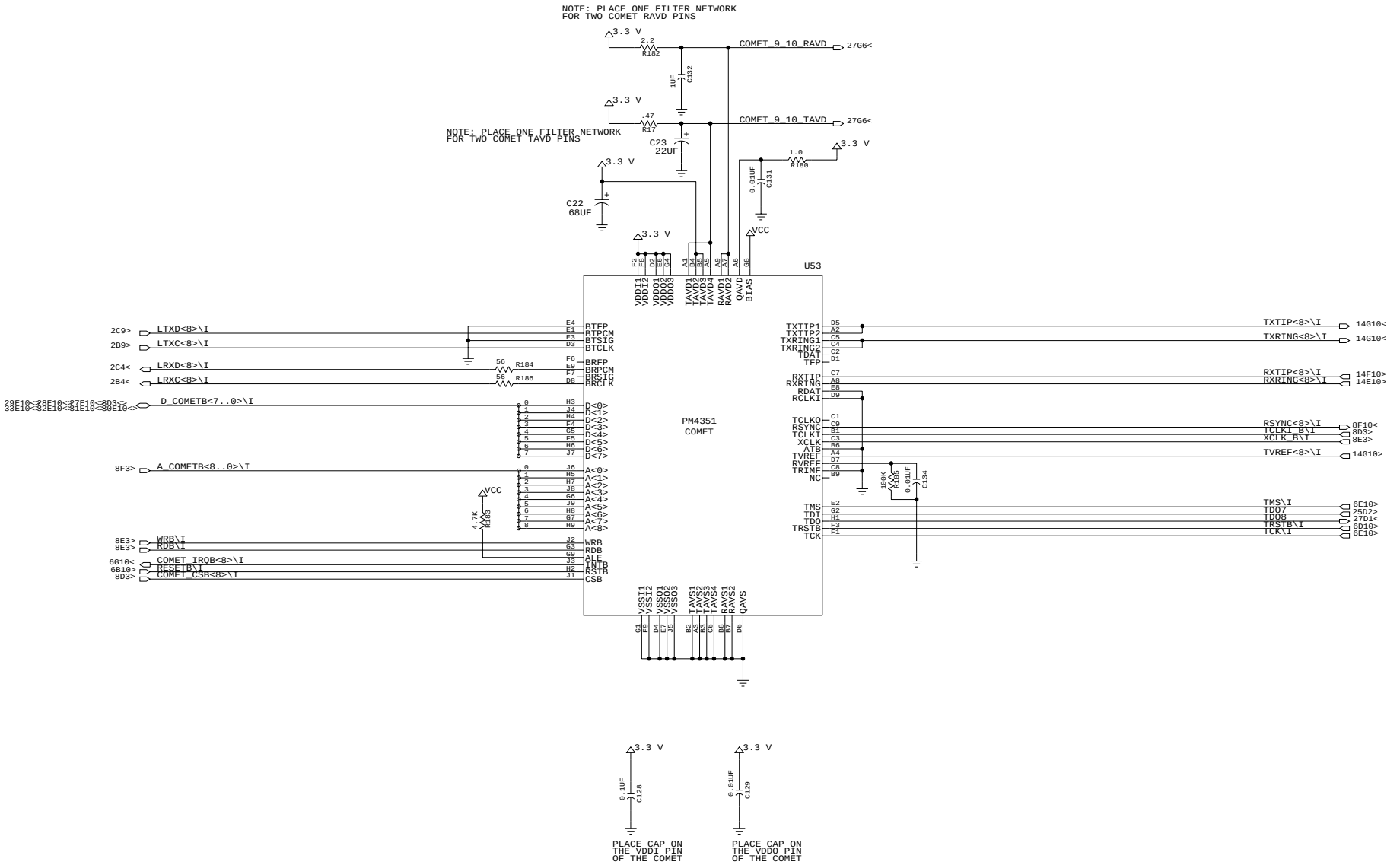
LAST_MODIFIED=Thu Sep 16 13:46:31 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 8	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:25 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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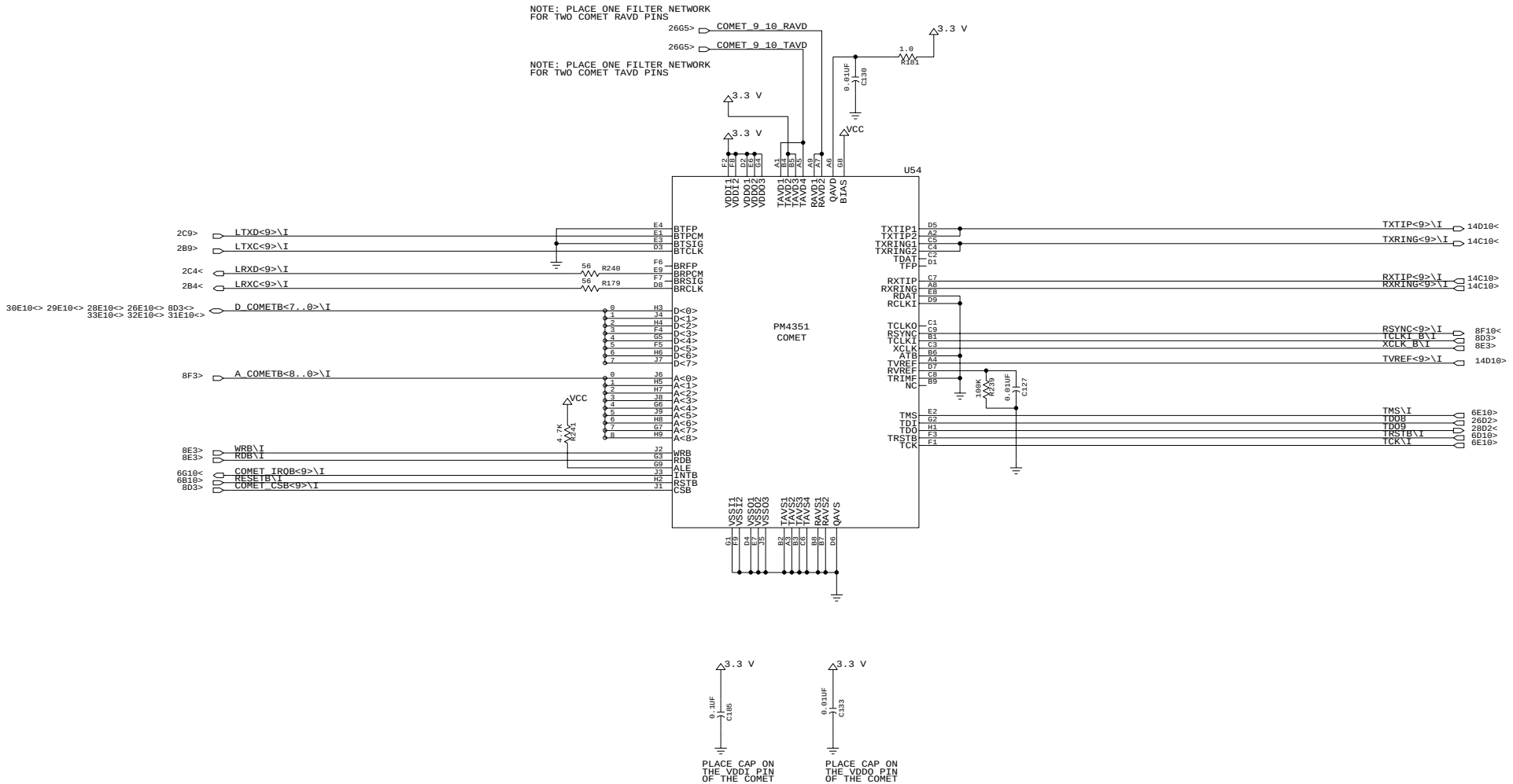
LAST_MODIFIED=Thu Sep 16 13:46:32 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 9	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:26 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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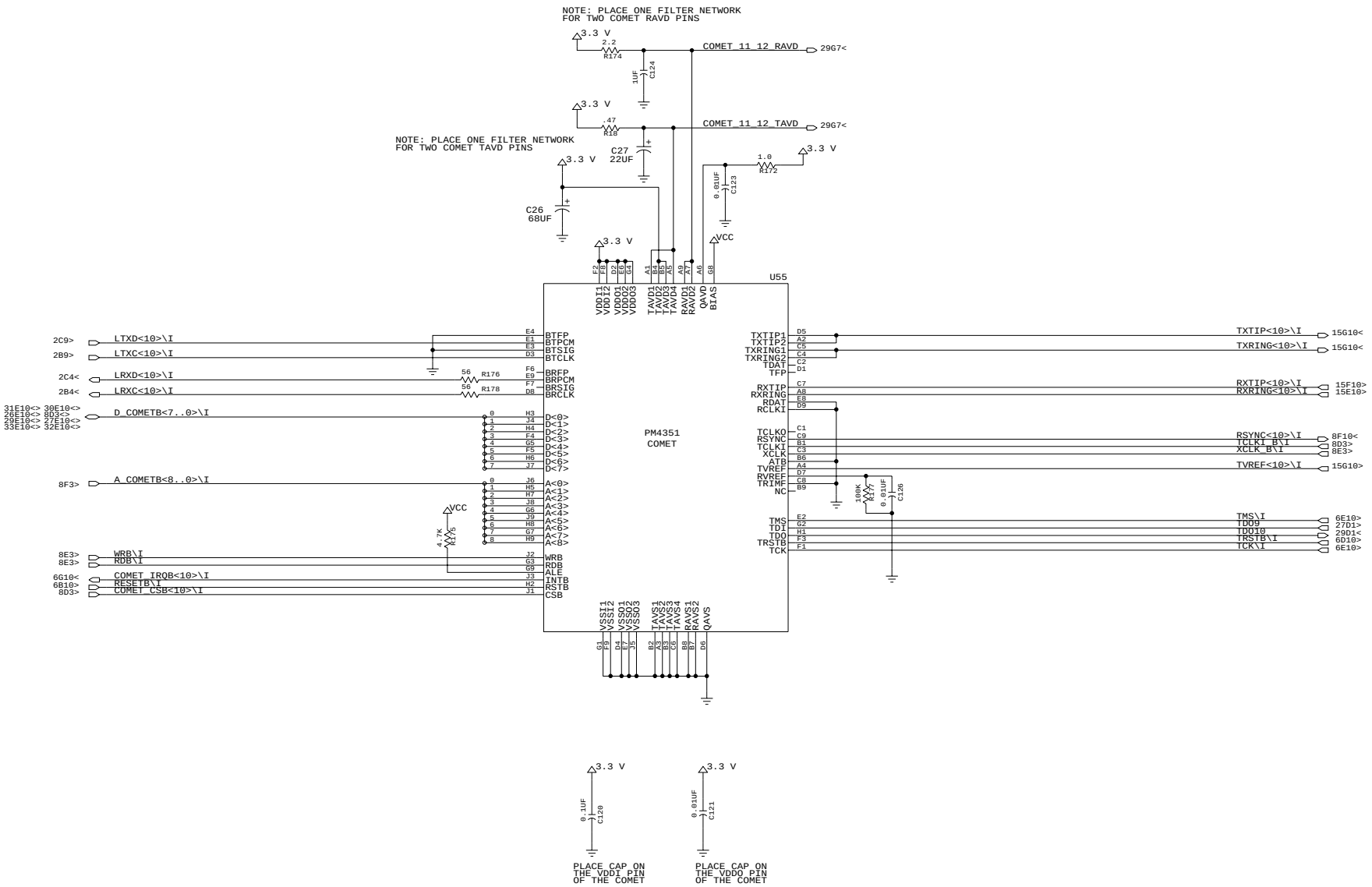
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 10	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:27 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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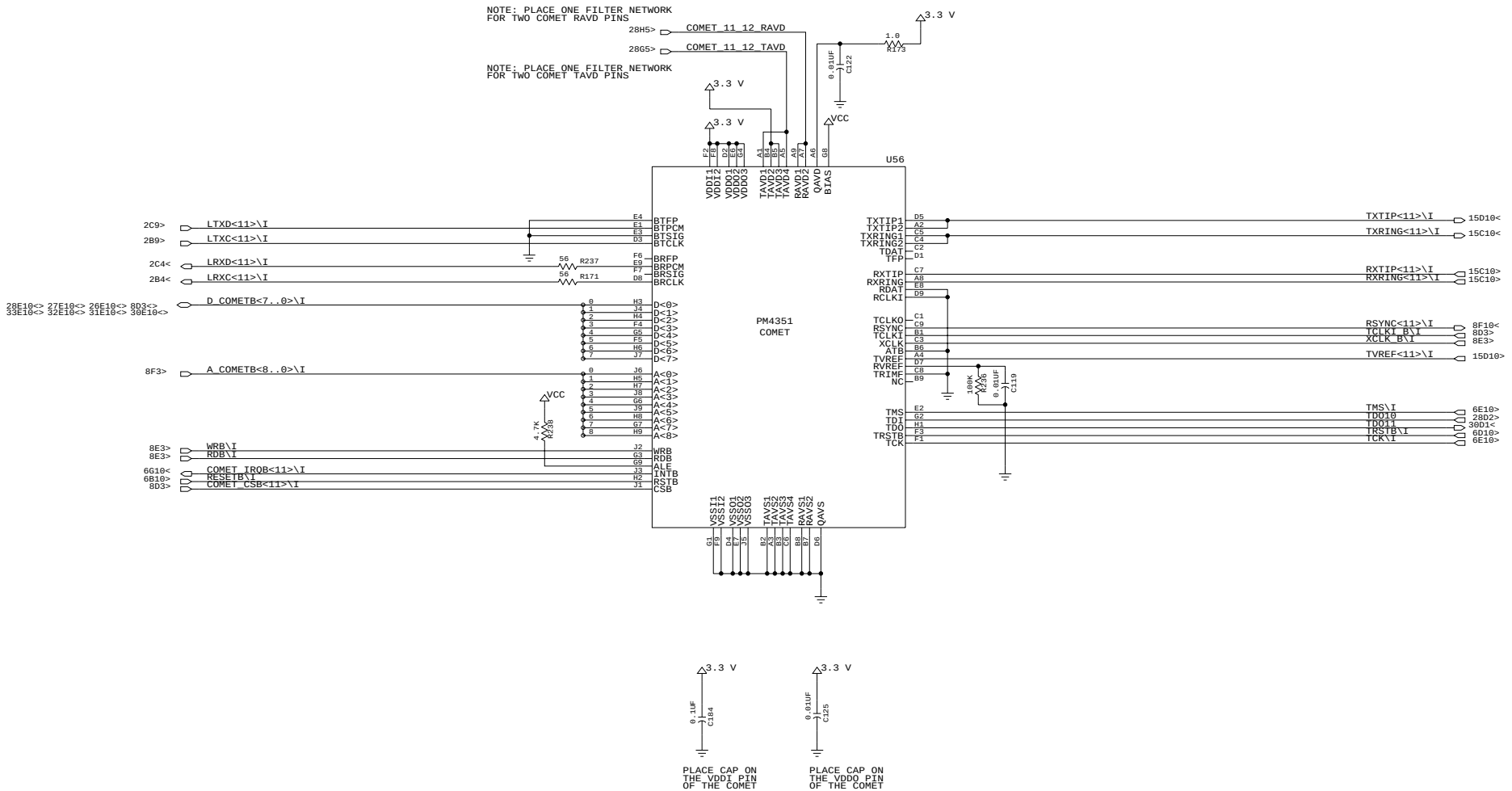
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 11	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:28 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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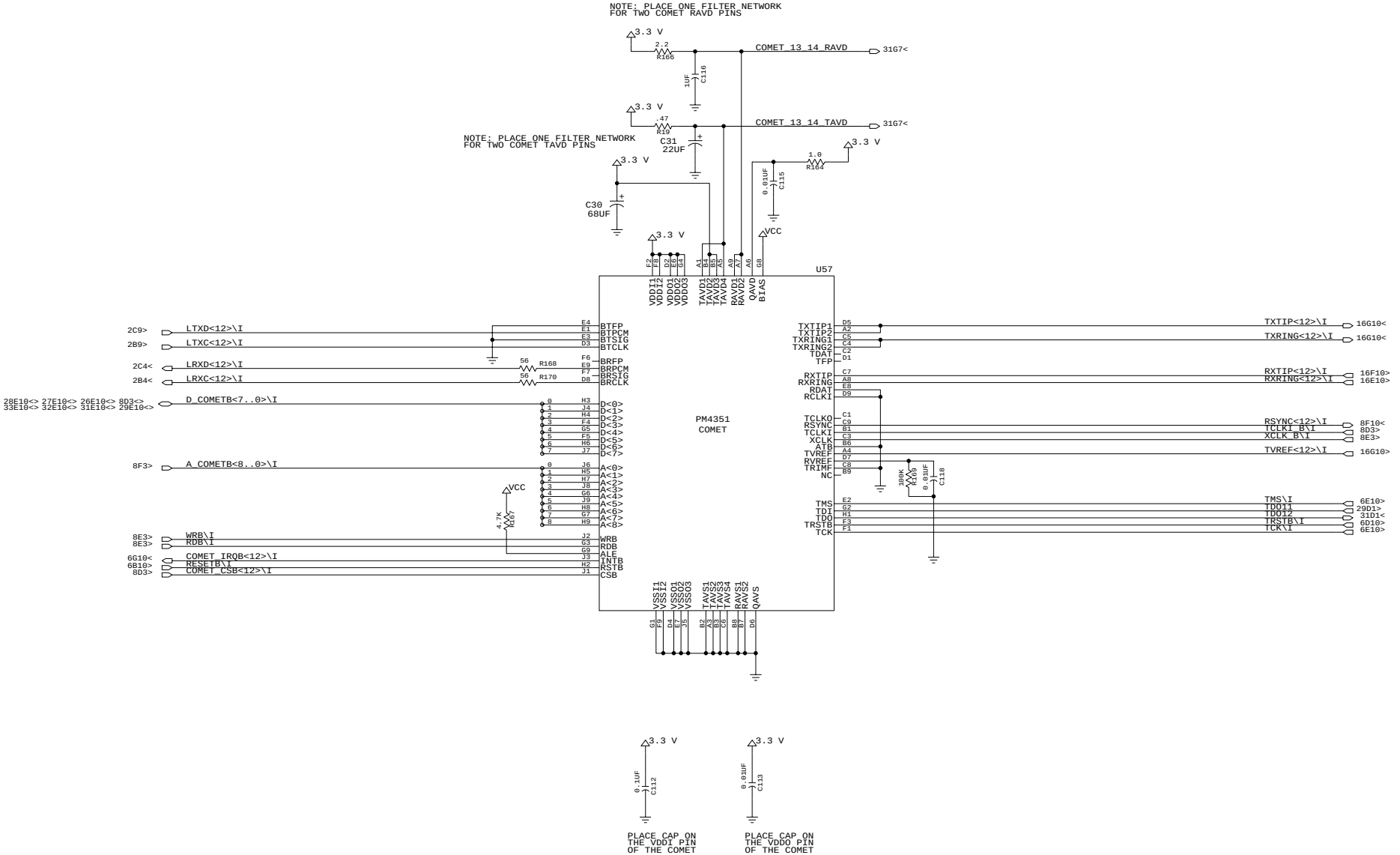
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 12	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:29 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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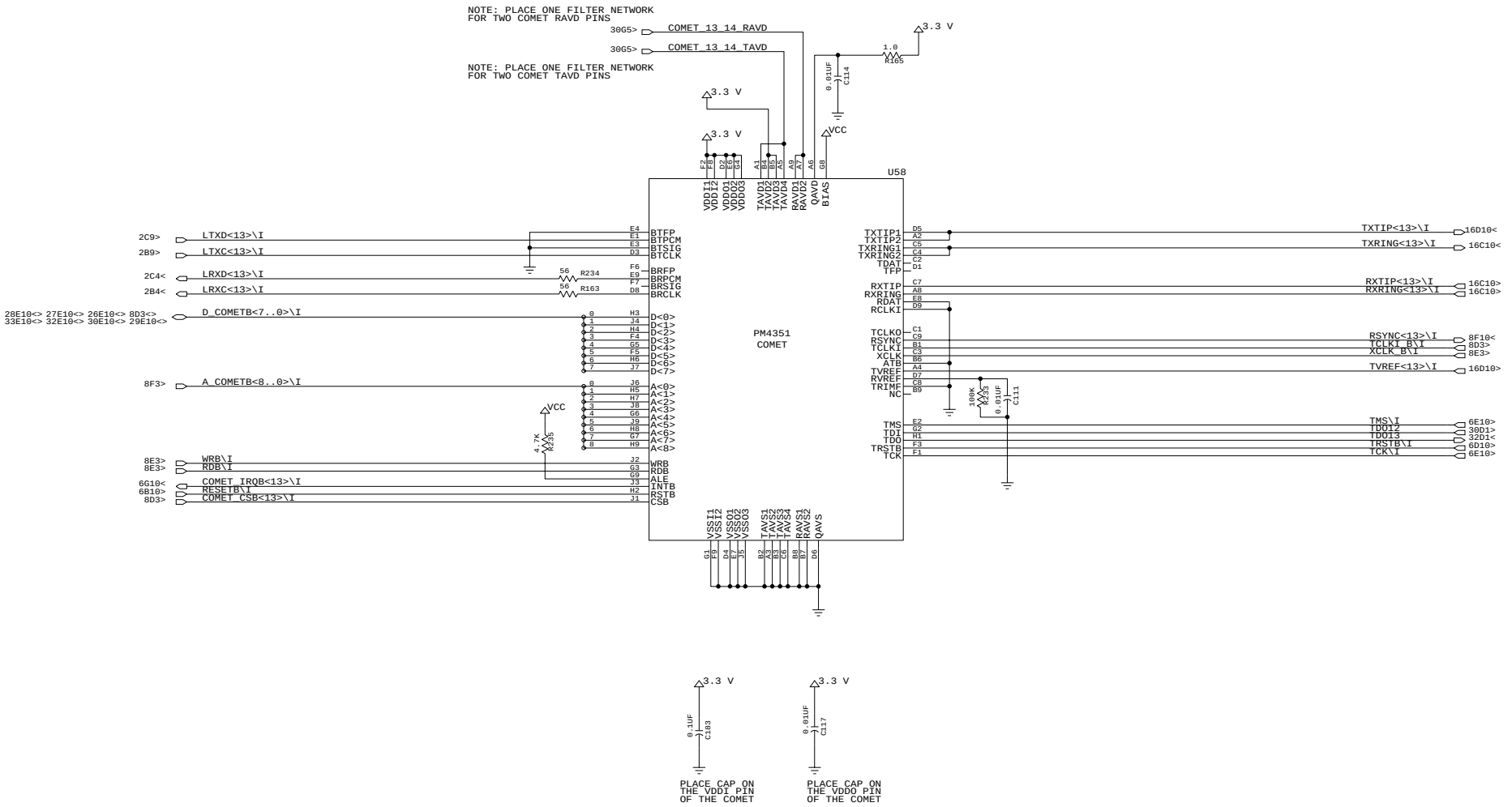
LAST_MODIFIED=Thu Sep 16 13:46:37 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 13	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:30 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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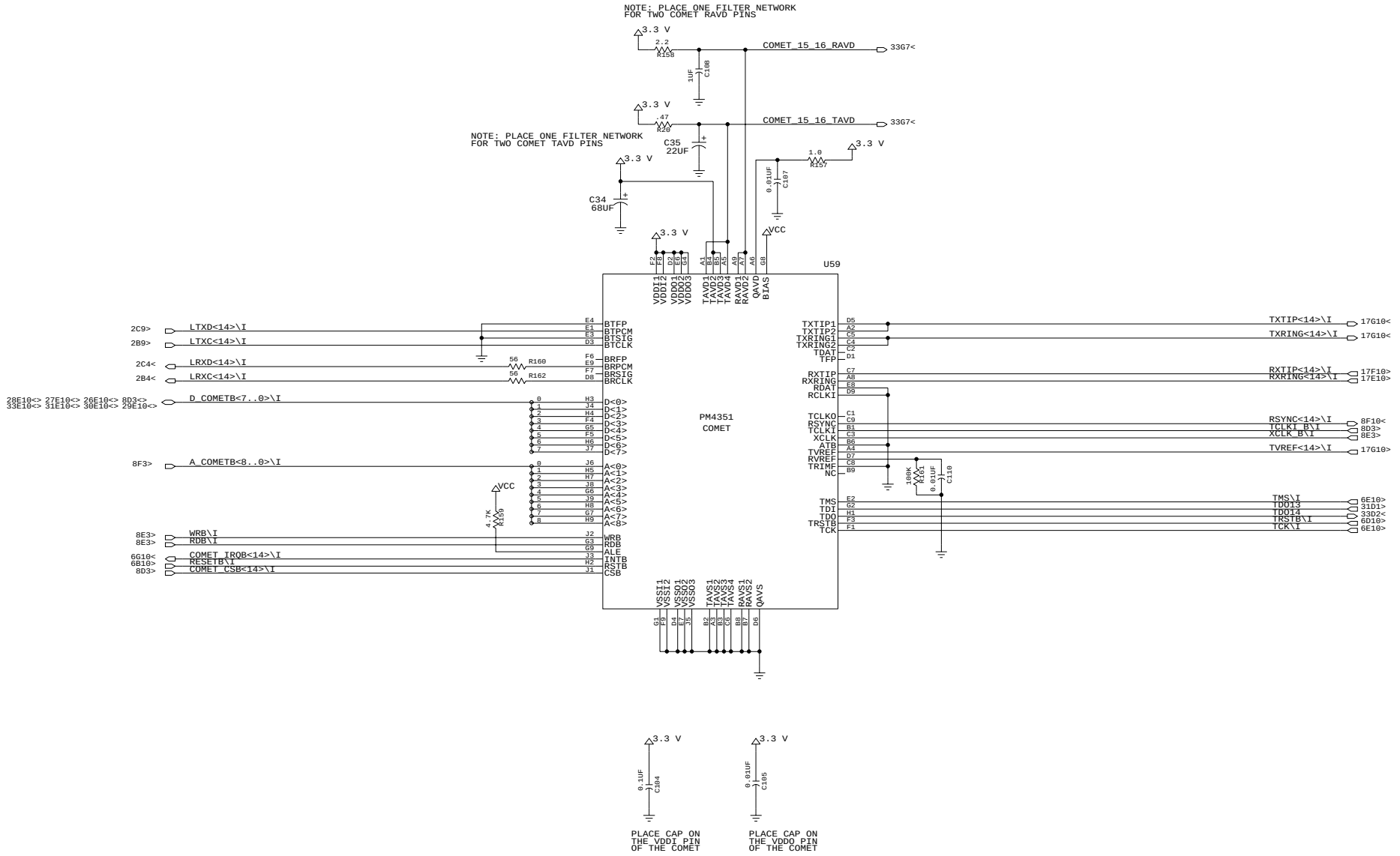
LAST_MODIFIED=Thu Sep 16 13:46:38 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 14	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:31 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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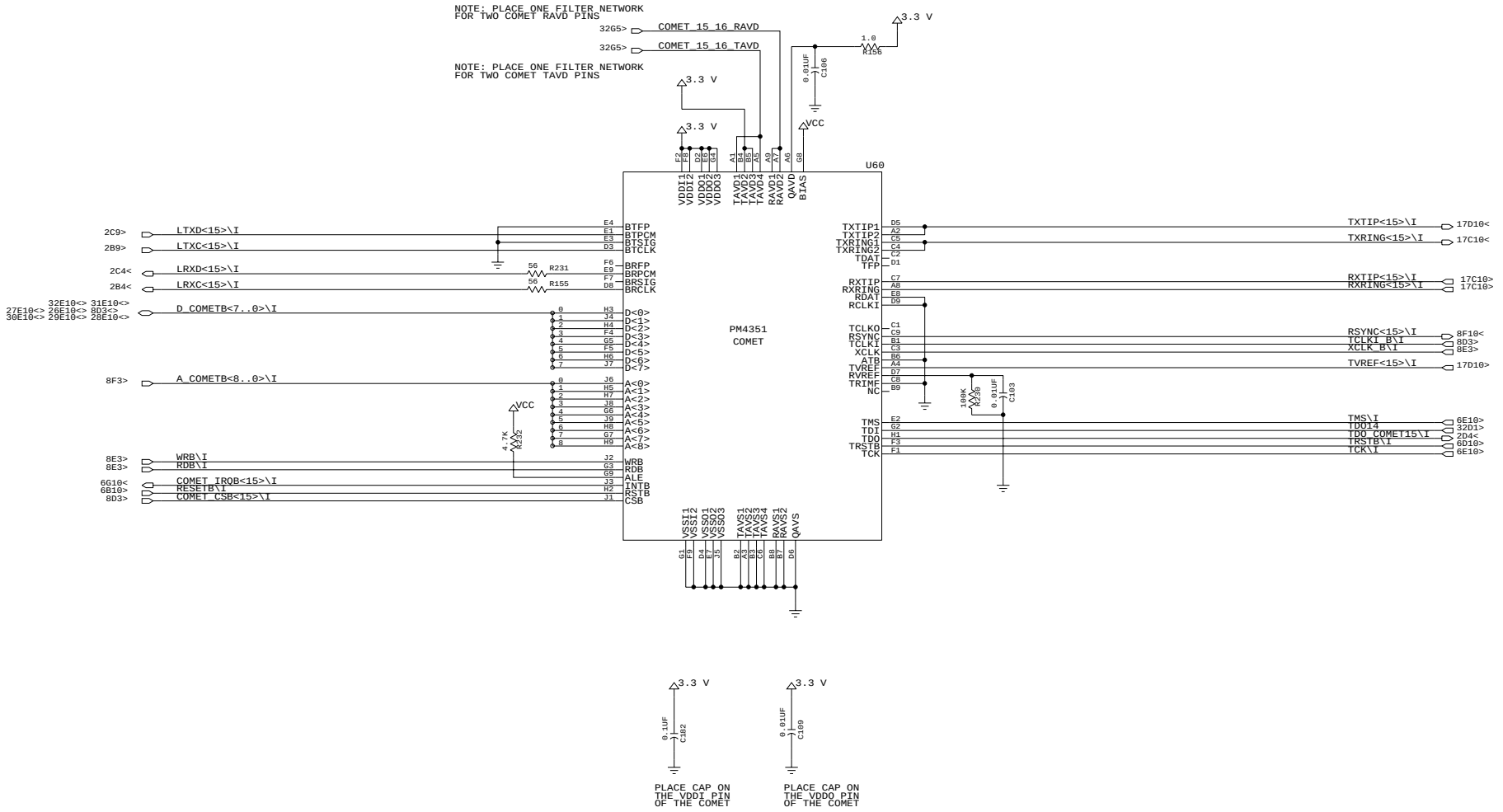
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 15	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:32 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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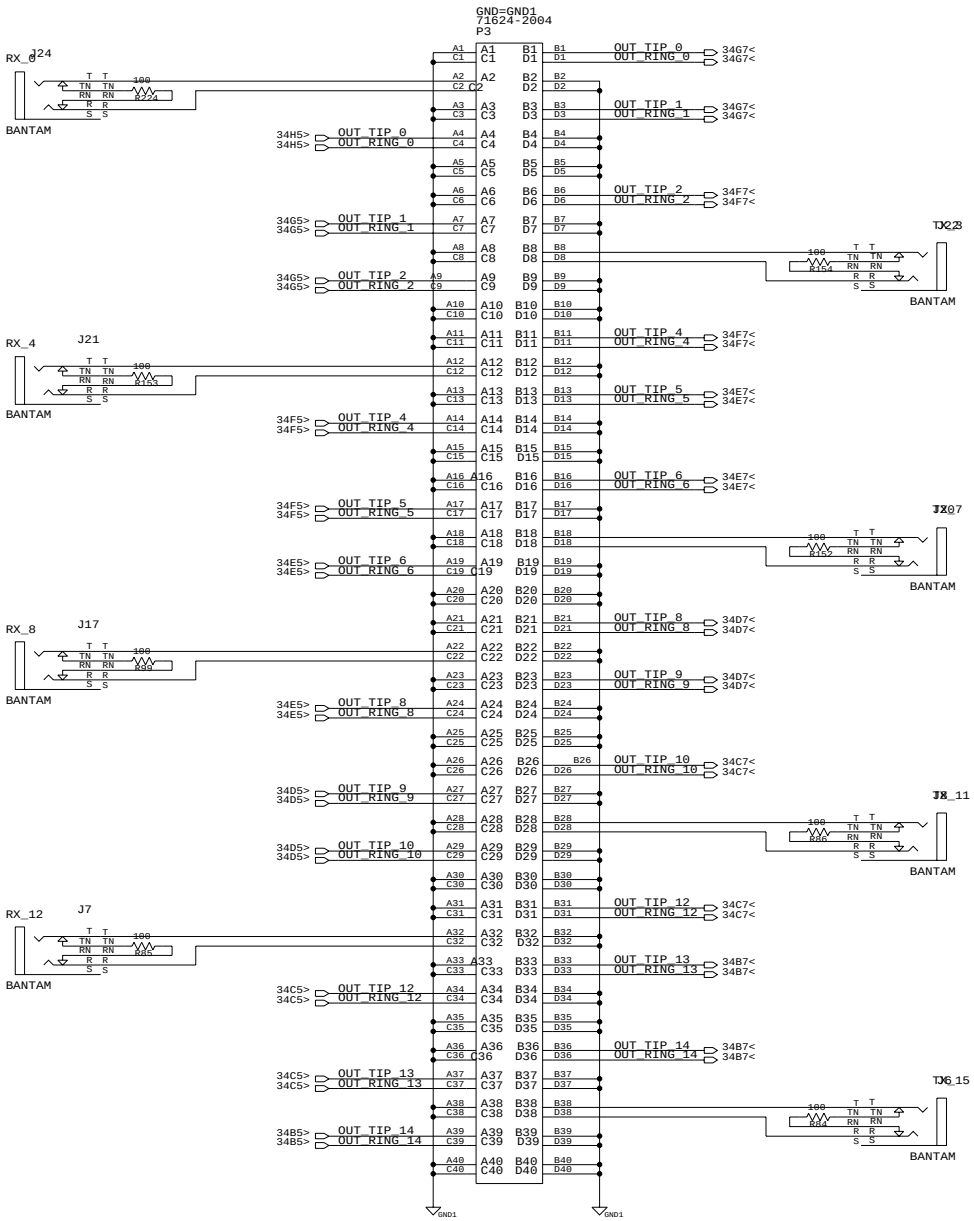
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD COMET BLOCK 16	DATE: 99/07/27
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:33 OF 33

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

TITLE=LOOPBACK_CARD
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LAST_MODIFIED=Thu Sep 16 13:46:12 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-990354	ISSUE: 1.0
TITLE: DSLAM LINE CARD LOOPBACK TEST JIG CARD	DATE: 99/08/20
ENGINEER: PMC-SIERRA, INC. (WT)	PAGE:34 OF 33

APPENDIX B: LAYOUT

This layout contains 13 pages as follows:

Sheet 1: Mechanical description

Sheet 2: Component Top

Sheet 3: Silkscreen Top

Sheet 4: Top Layer

Sheet 5: GND Plane

Sheet 6: VCC Plane

Sheet 7: Sig1 Layer

Sheet 8: Sig2 Layer

Sheet 9: 3V3 Plane

Sheet 10: GND Plane

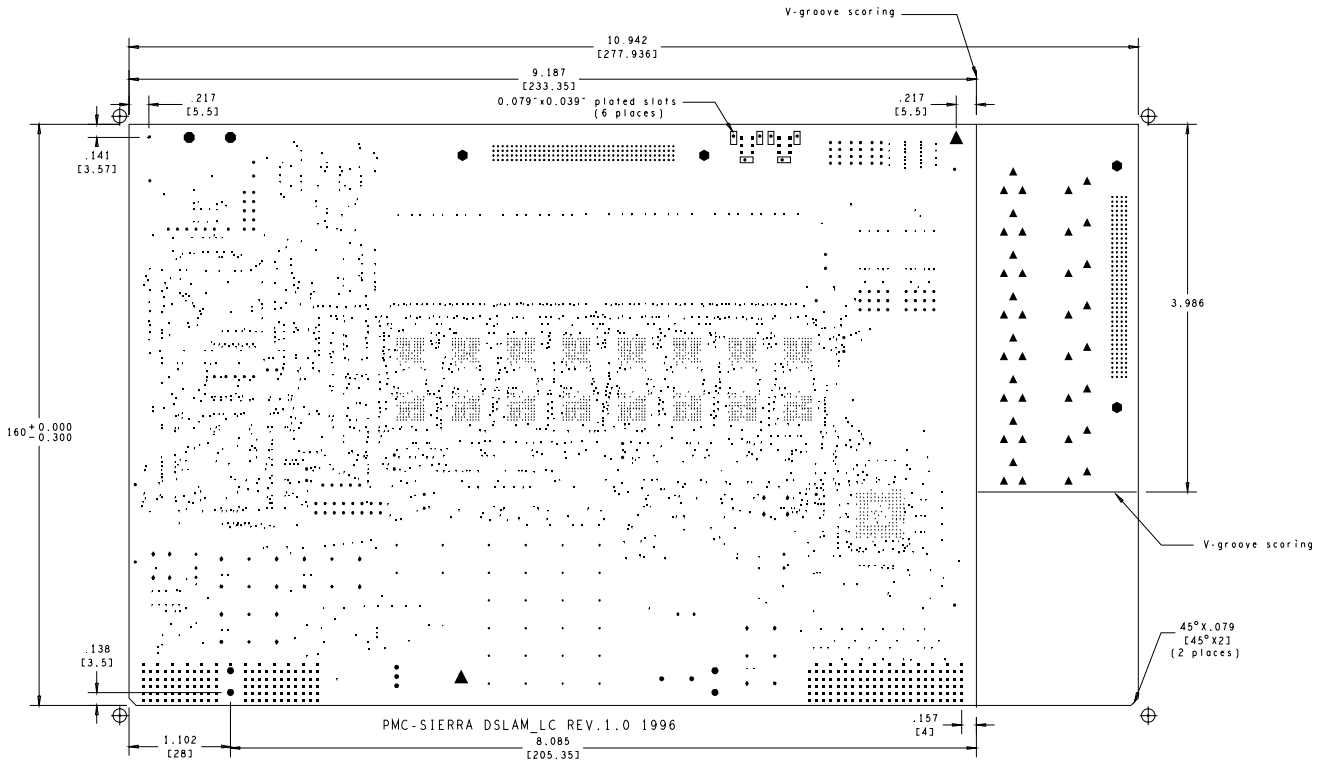
Sheet 11: Bottom Layer

Sheet 12: Component Bottom

Sheet 13: Silkscreen Bottom

The PCB was designed to have the Loopback Test Jig card as a breakout of the board.

REVISIONS				
REV	DESCRIPTION	DATE YY MM DD	APPROVED	



	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	--------
	FR-4	DIELECTRIC	--------	--------	6 mil	4.5
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	3 mil	4.5
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	12 mil	4.5
#	COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	10 mil	4.5
#	COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	12 mil	4.5
	COPPER	CONDUCTOR	3V3_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	3 mil	4.5
	COPPER	CONDUCTOR	GND1_PLANE	POSITIVE	1.44 mil	--------
	FR-4	DIELECTRIC	--------	--------	6 mil	4.5
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	--------

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	12.0	PLATED	1250
·	13.0	PLATED	1873
·	23.0	PLATED	320
·	25.0	PLATED	28
▪	25.0	PLATED	244
▪	32.0	PLATED	12
·	36.0	PLATED	119
·	39.0	PLATED	6
·	39.37	PLATED	2
·	42.0	PLATED	8
·	42.0	PLATED	4
·	42.0	PLATED	20
▲	50.0	PLATED	40
•	55.0	PLATED	5
⬢	125.0	PLATED	4
·	149.606	PLATED	1
▲	150.0	PLATED	1
•	78.74	NOT PLATED	4
●	128.0	NOT PLATED	2
▲	150.0	NOT PLATED	1

Note: 50 ohm controlled impedance traces with trace width of 10 mil are on all signal layers.

Note: 75 ohm controlled impedance traces with trace width of 5 mil are on all signal layers.

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
SIG1
SIG2
3V3 PLANE
GND1 PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING
ASSY TOP
ASSY BOTTOM

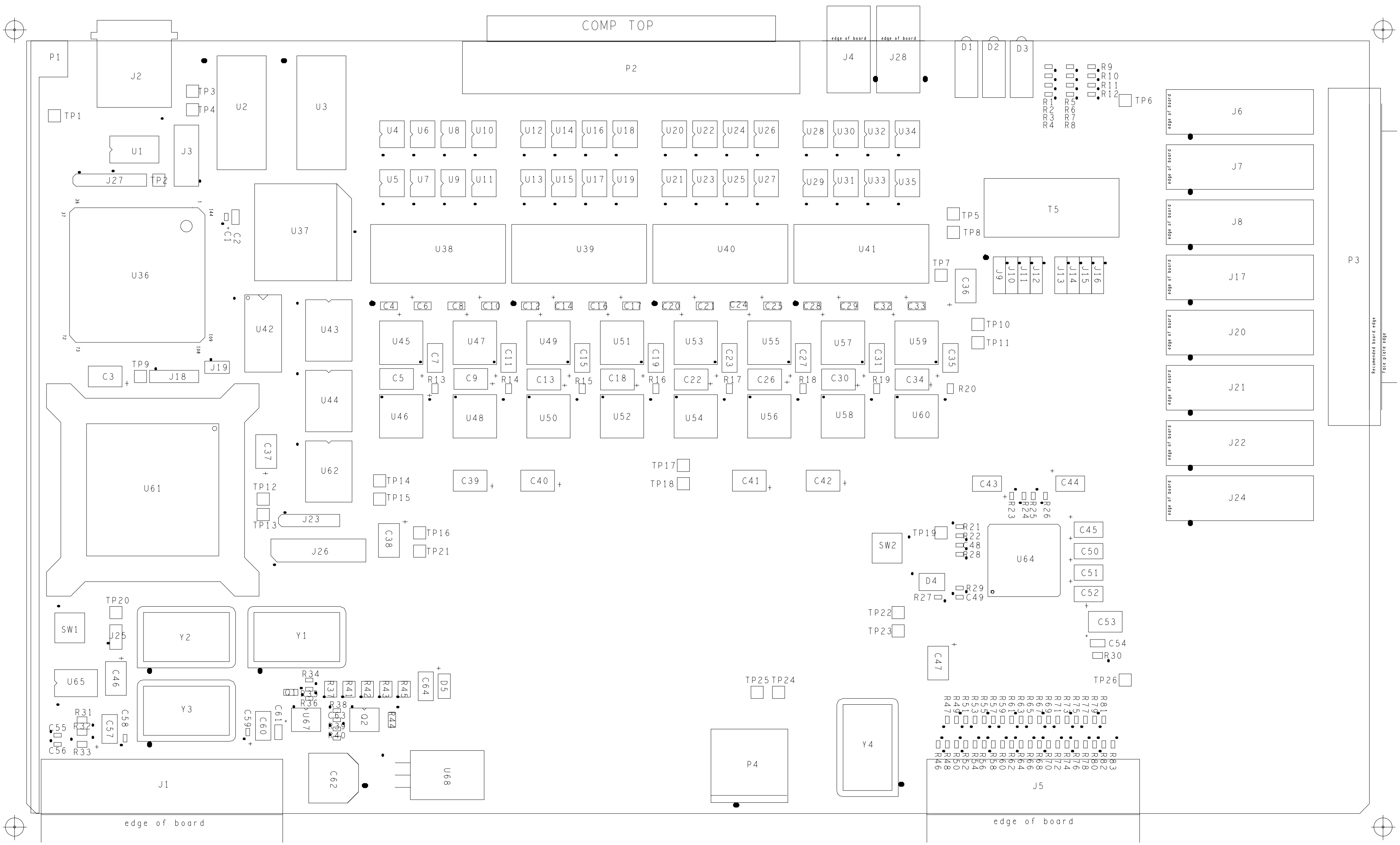
UNLESS OTHERWISE SPECIFIED		DATE YY MM DD
DIMENSIONS ARE IN INCHES	DRAWN	
TOLERANCES ON:		
2 PL DECIMALS ±	CHECKED	
3 PL DECIMALS ±	ENGRG	
ANGLES ±	ISSUED	
FRACTIONS ±		

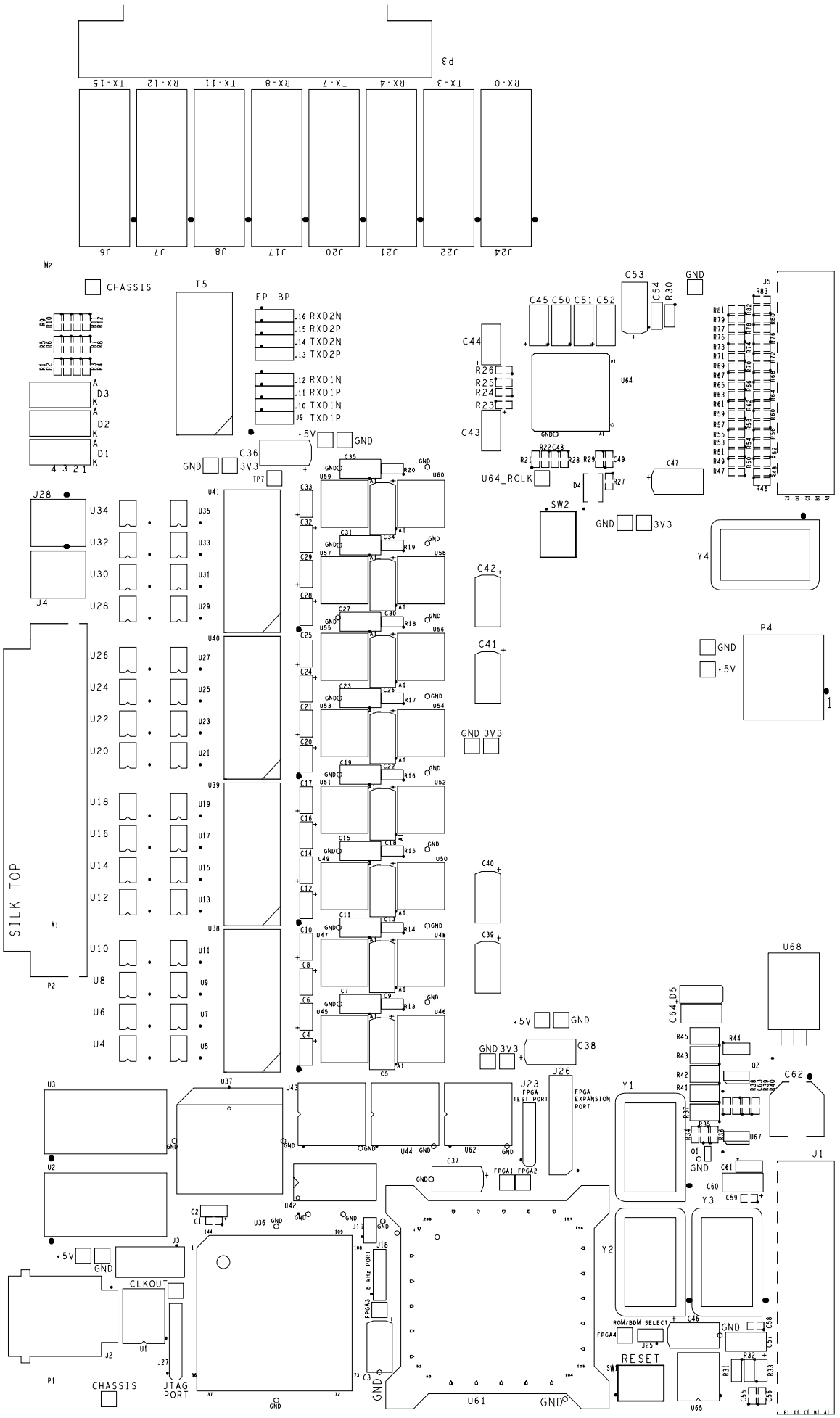
PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF


COMP TOP
P1
J2
P2
J4
J28
edge of board
D1
D2
D3
R9
R10
R11
R12
R1
R2
R3
R4
R5
R6
R7
R8
TP6
TP1
TP3
TP4
U1
J3
U2
U3
U4
U6
U8
U10
U12
U14
U16
U18
U20
U22
U24
U26
U28
U30
U32
U34
J6
J27
TP2
U5
U7
U9
U11
U13
U15
U17
U19
U21
U23
U25
U27
U29
U31
U33
U35
J7
U36
C1
C2
U37
T5
TP5
TP8
J8
U38
U39
U40
U41
TP7
C36
J9
J10
J11
J12
J13
J14
J15
J16
J17
P3
C4
C6
C8
C10
C12
C14
C16
C17
C20
C21
C24
C25
C28
C29
C32
C33
U42
U43
U45
U47
U49
U51
U53
U55
U57
U59
TP10
TP11
J20
C7
C11
C15
C19
C23
C27
C31
C35
TP9
C3
J18
J19
C5
R13
C9
R14
C13
R15
C18
R16
C22
R17
C26
R18
C30
R19
C34
R20
J21
U44
U46
U48
U50
U52
U54
U56
U58
U60
U61
C37
U62
J22
TP17
TP18
TP14
TP15
C39
C40
C41
C42
C43
C44
R23
R24
R25
R26
J24
TP12
TP13
J23
C38
TP16
TP21
J26
SW2
TP19
R21
R22
C48
R28
U64
C45
C50
C51
C52
D4
R27
R29
C49
TP22
TP23
C53
C54
R30
TP20
SW1
J25
Y2
Y1
C47
C46
U65
R34
Q1
R35
R36
R37
R41
R42
R43
R45
C64
D5
TP25
TP24
TP26
R31
R32
C55
C56
R33
C57
C58
Y3
C59
C60
C61
U67
R38
C63
R39
R40
Q2
R44
Y4
R47
R49
R51
R53
R55
R57
R59
R61
R63
R65
R67
R69
R71
R73
R75
R77
R79
R81
R46
R48
R50
R52
R54
R56
R58
R60
R62
R64
R66
R68
R70
R72
R74
R76
R78
R80
R82
R83
J1
C62
U68
P4
J5
edge of board
edge of board


P3
RX-0
TX-3
RX-4
TX-7
RX-8
TX-11
RX-12
TX-15
J24
J22
J21
J20
J17
J8
J7
J6
W2
CHASSIS
T5
FP BP
J16 RXD2N
J15 RXD2P
J14 TXD2N
J13 TXD2P
J12 RXD1N
J11 RXD1P
J10 TXD1N
J9 TXD1P
+5V
GND
C36
3V3
TP7
J28
J4
J5
R83
C45 C50 C51 C52
C53
C54
R30
C44
R26
R25
R24
R23
C43
U64
U64_RCLK
C47
D4
R27
SW2
GND 3V3
Y4
C42
C41
GND 3V3
P4
GND
+5V
1
SILK TOP
A1
P2
C40
C39
C38
GND 3V3
+5V
GND
U68
C64_D5
R45
R44
R43
R42
R41
Q2
C62
R37
R35
U67
Q1
GND
C61
C60
C59
Y3
J1
U3
U37
U43
J23
FPGA TEST PORT
J26
FPGA EXPANSION PORT
Y1
U2
U42
U44
U62
C37
FPGA1
FPGA2
C2
C1
U36
J19
J18
FPGA3
8 kHz PORT
Y2
J3
+5V
GND
CLKOUT
U1
J2
P1
J27
JTAG PORT
CHASSIS
C3
GND
U61
GND
ROM/BDM SELECT
FPGA4
J25
C48
GND
C57
C58
RESET
SW1
R32
R31
R33
U65
C55
C56
U41
U40
U39
U38
U35
U33
U31
U29
U27
U25
U23
U21
U19
U17
U15
U13
U11
U9
U7
U5
U34
U32
U30
U28
U26
U24
U22
U20
U18
U16
U14
U12
U10
U8
U6
U4
C35
C33
C32
C31
C34
C29
C28
C27
C30
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C24
C23
C26
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C4
C5
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U48
U47
U46
U45
R20
R19
R18
R17
R16
R15
R14
R13
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R21
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R29
C49
R46
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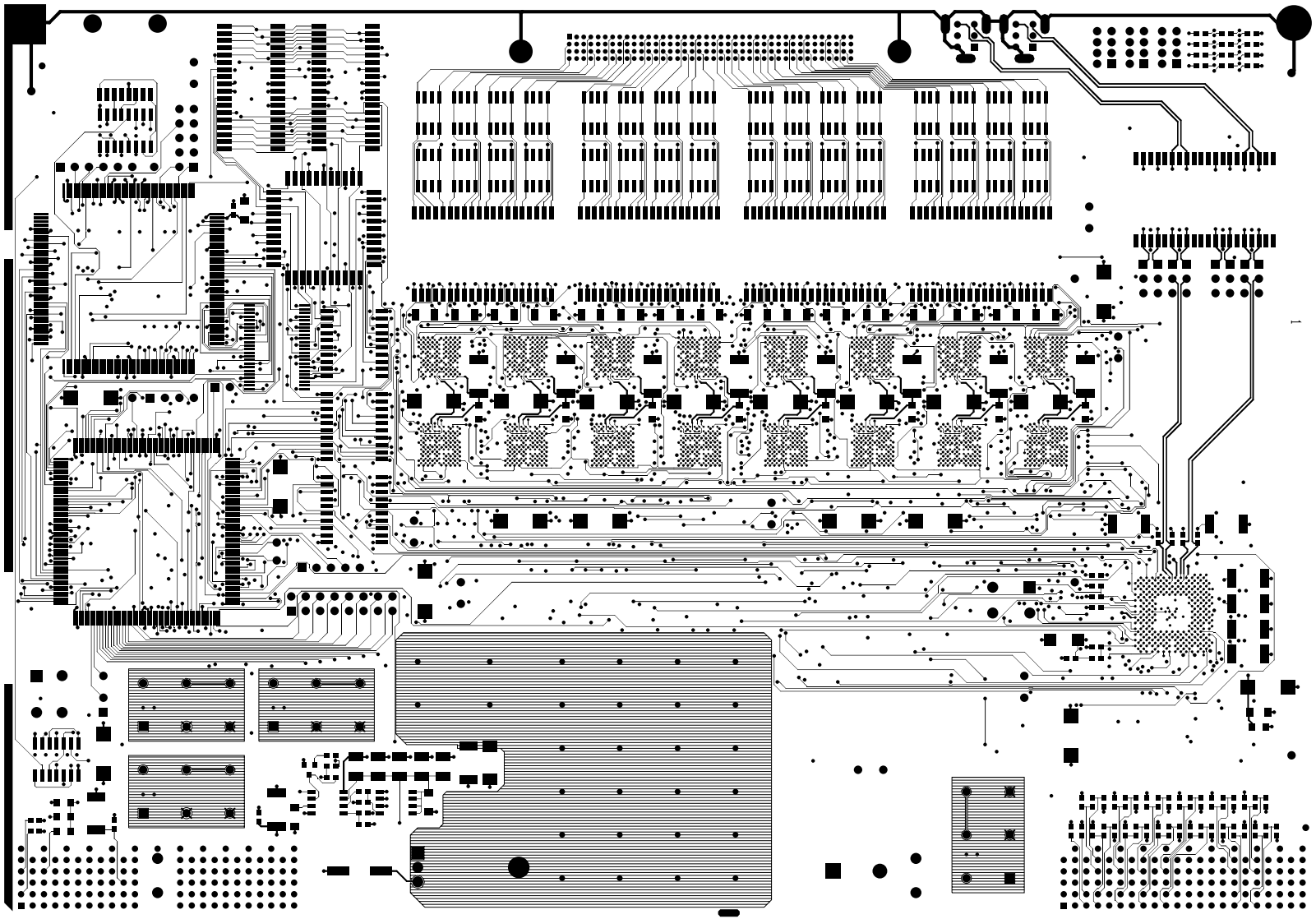
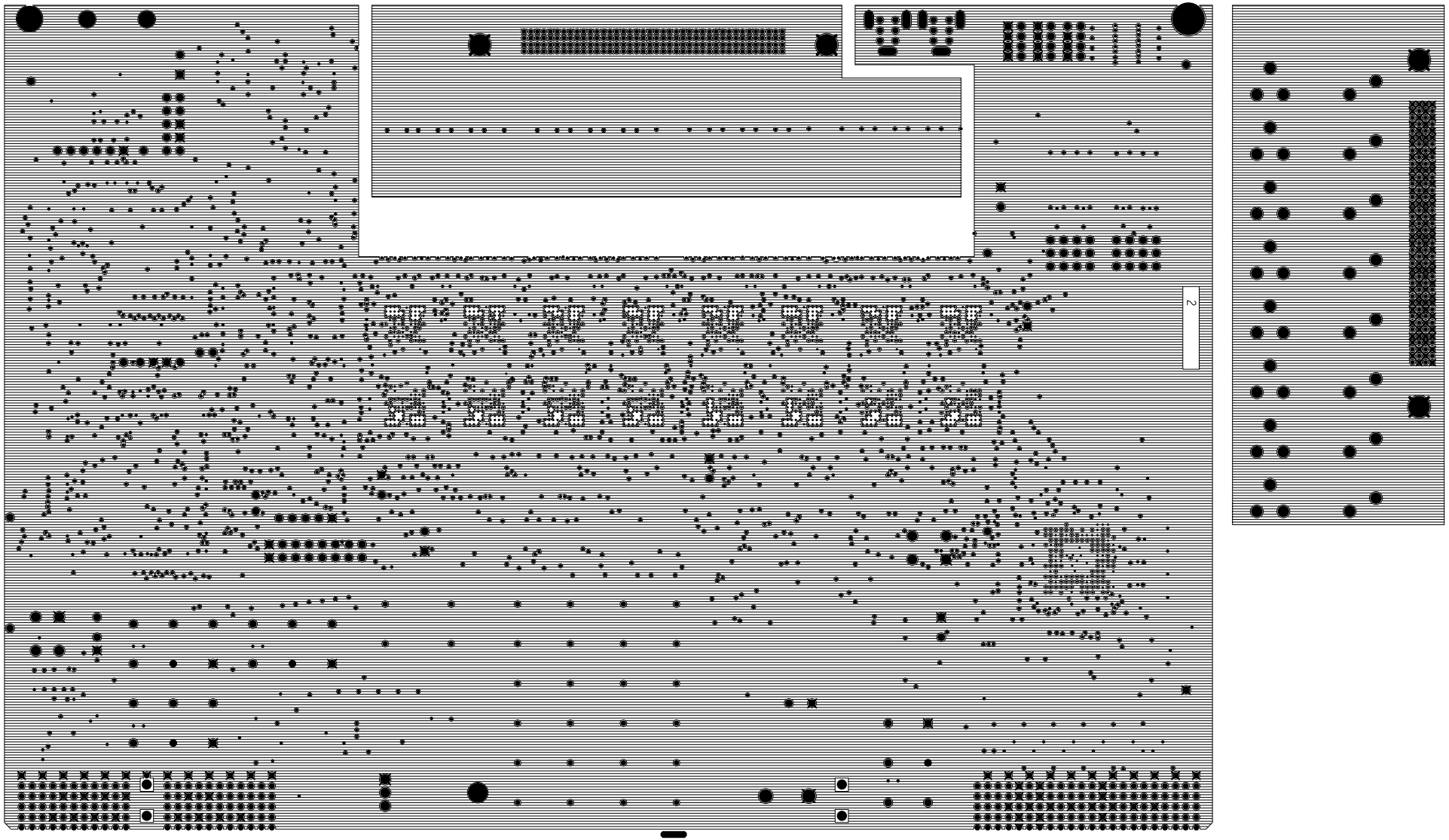
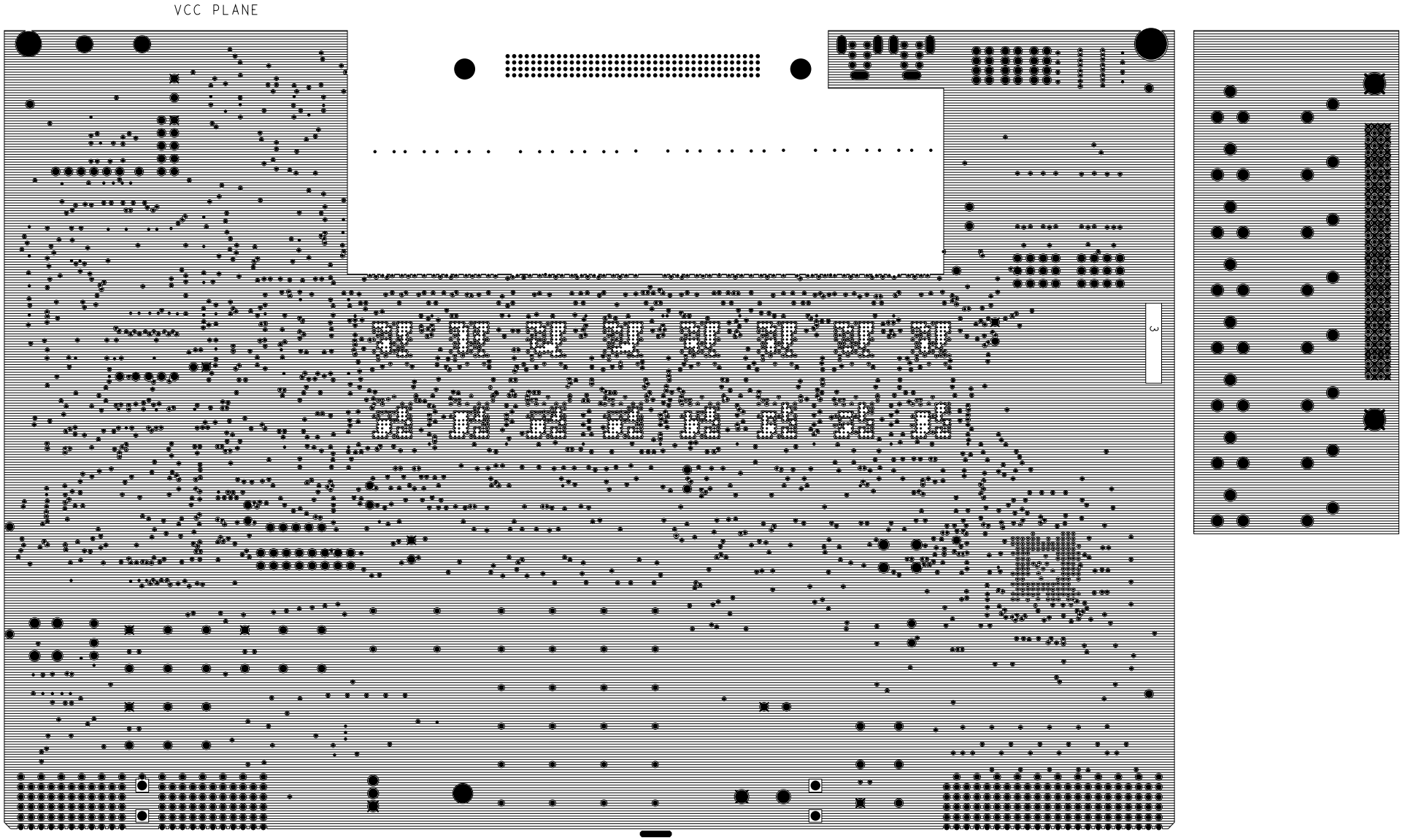
R79
R80
R81
R82
R9
R10
R11
R12
R5
R6
R7
R8
R1
R2
R3
R4
A
D3
K
A
D2
K
A
D1
K
4 3 2 1

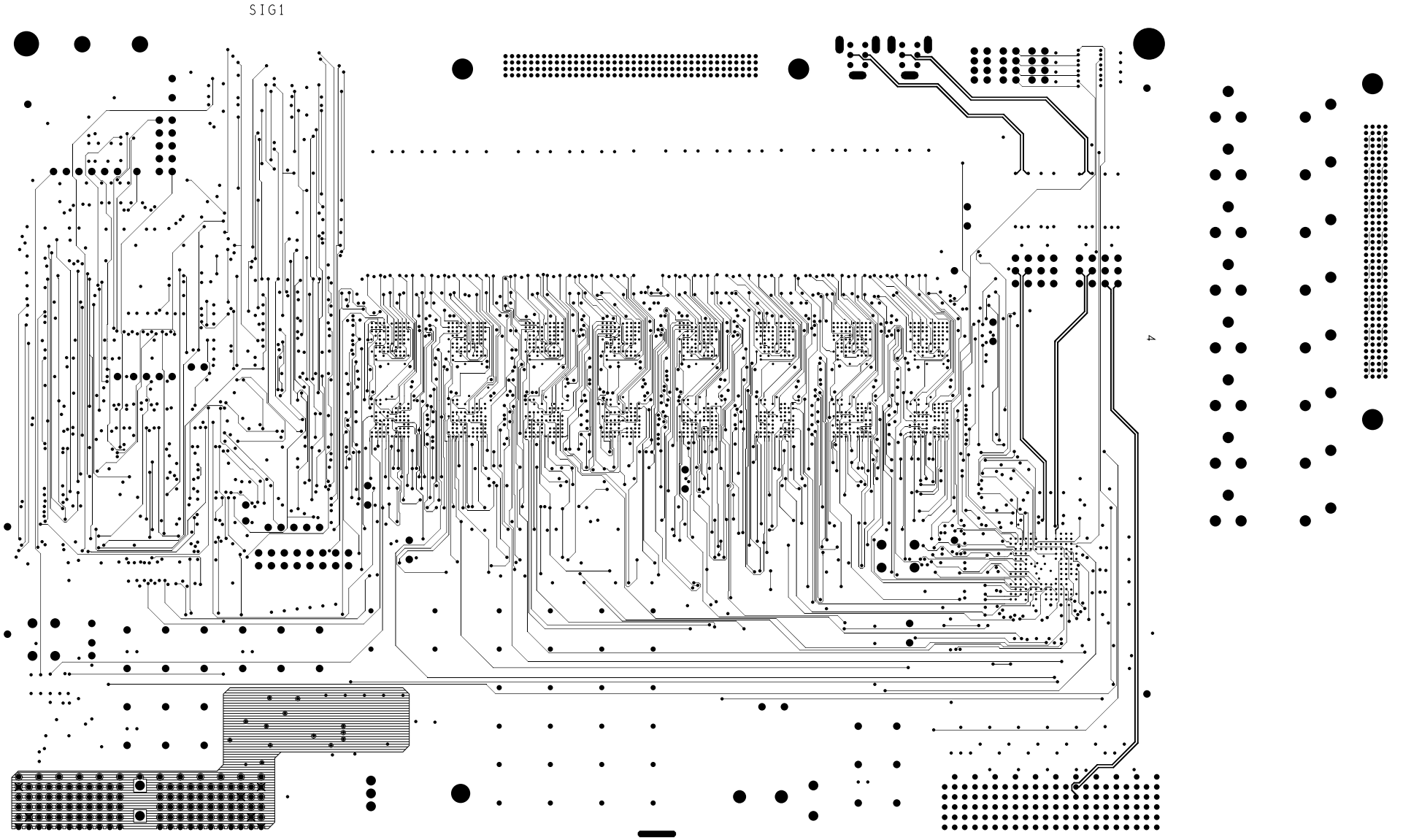
TOP LAYER

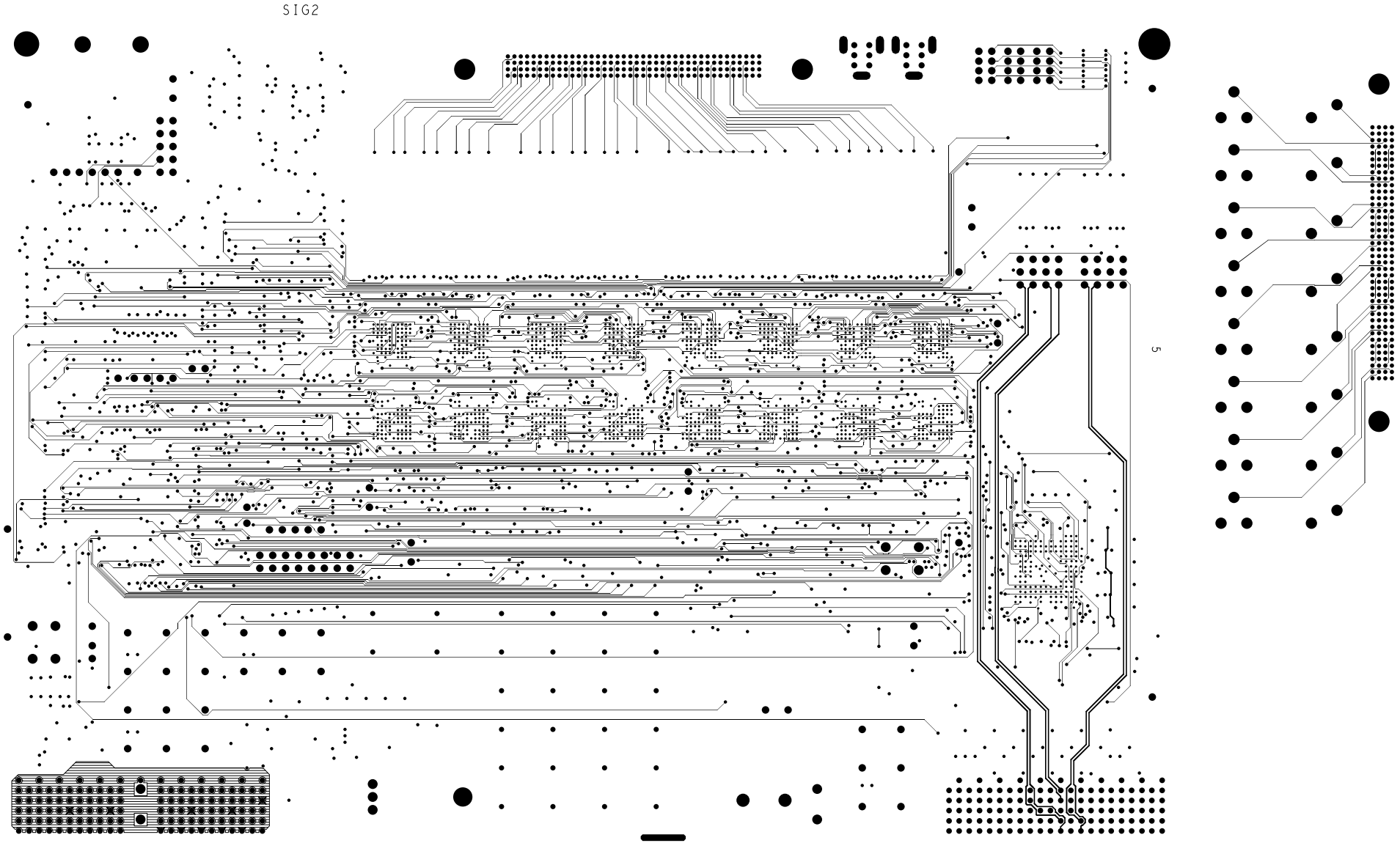


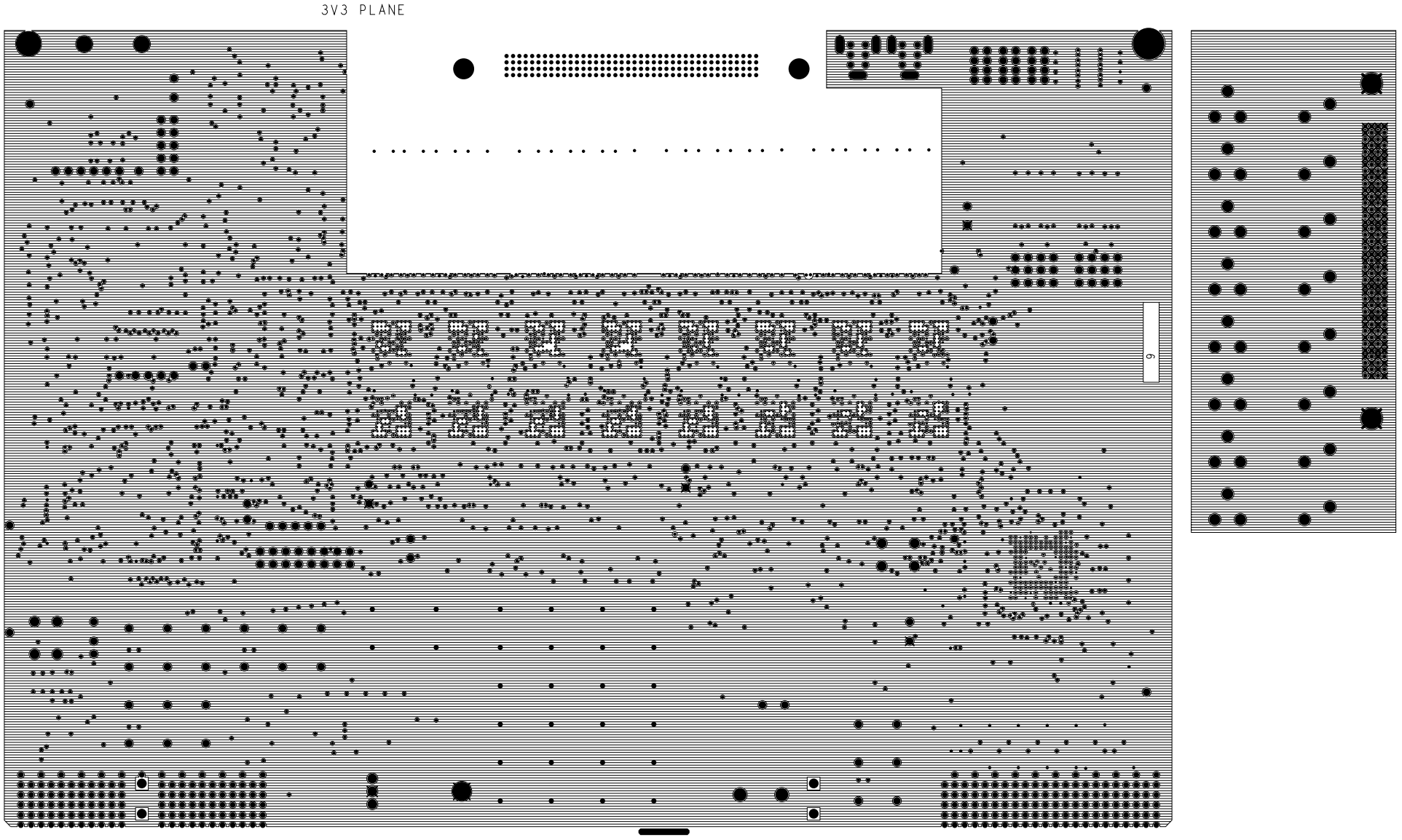
GND PLANE



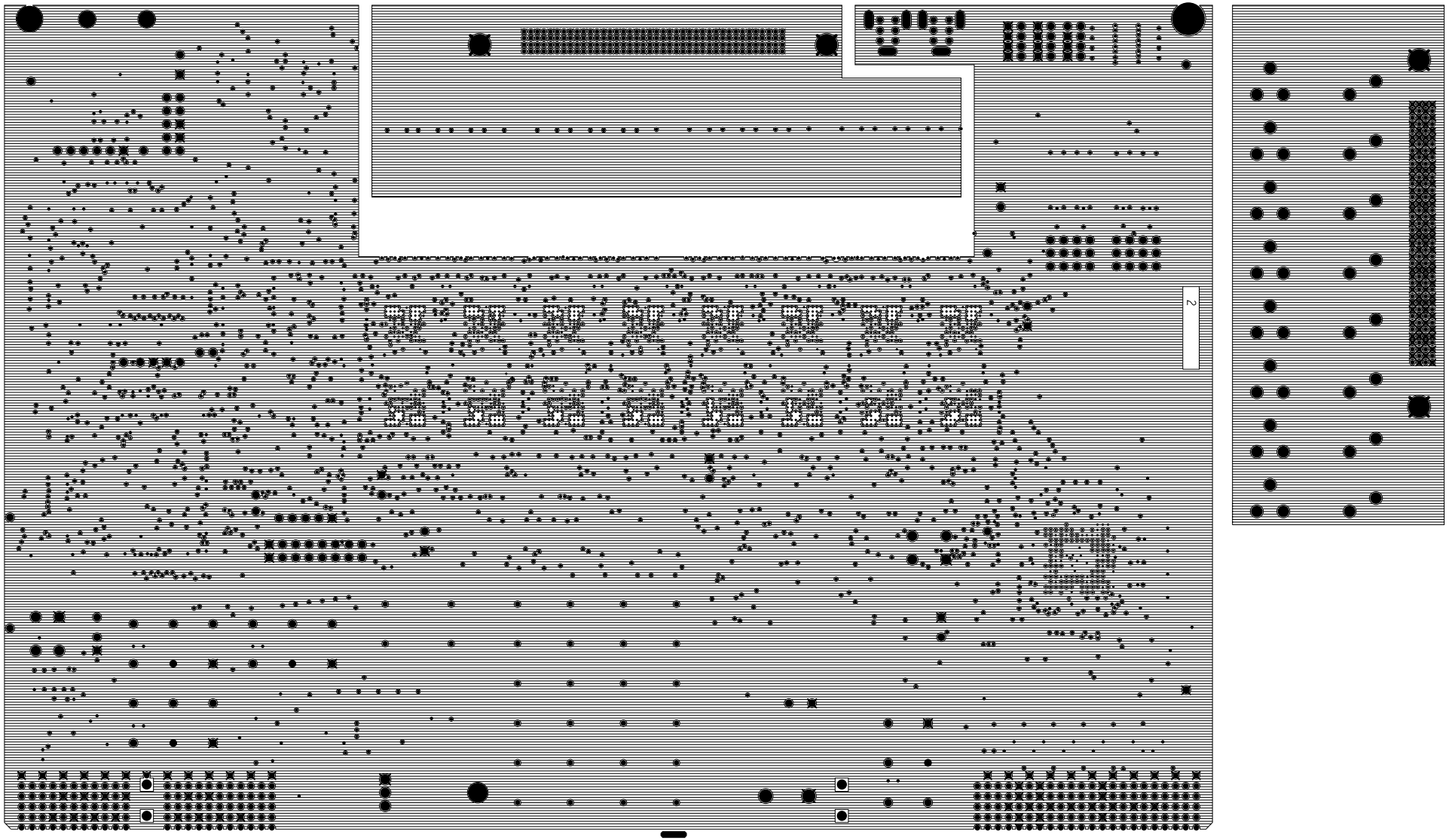

VCC PLANE
3


SIG1
4

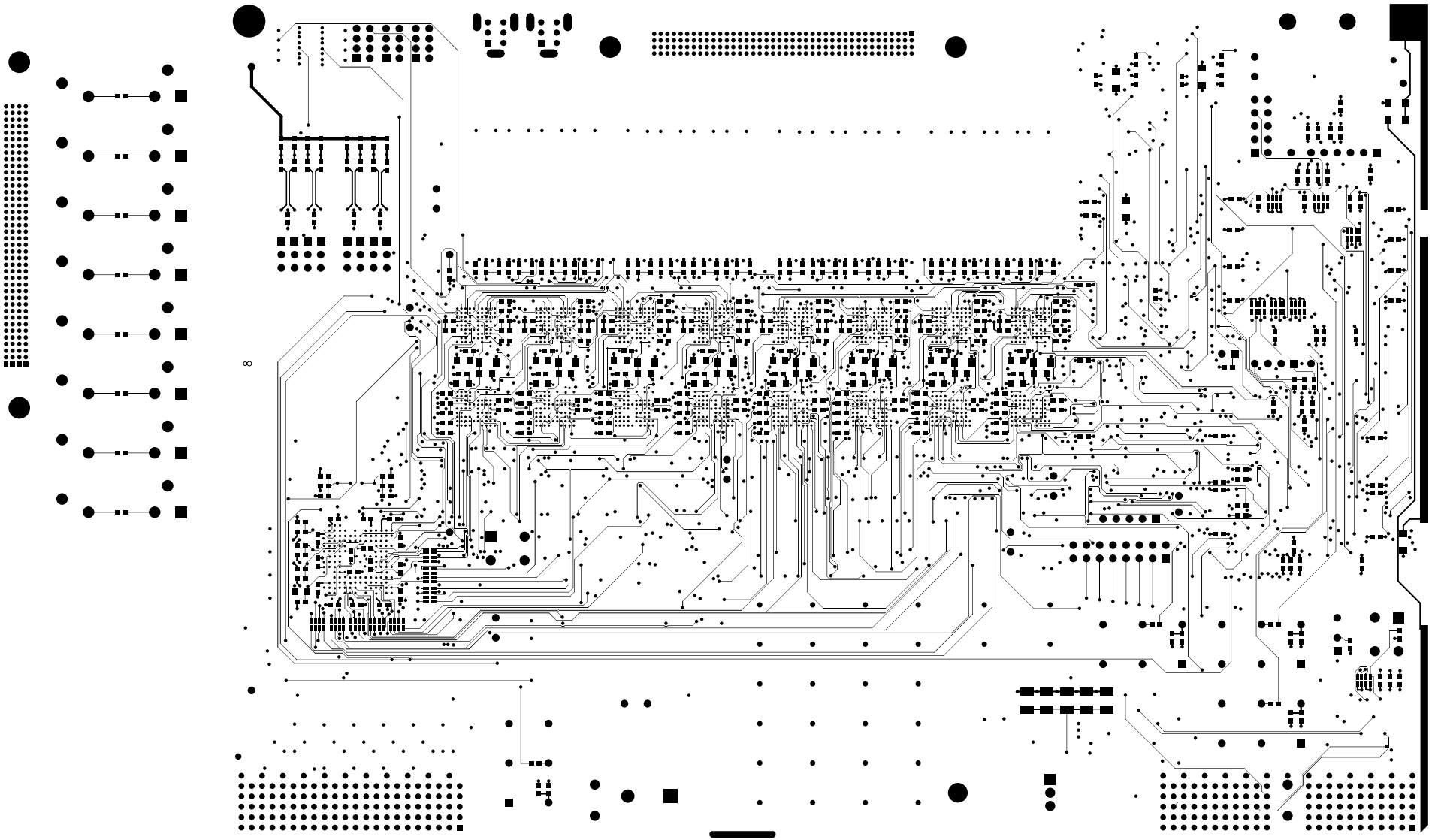

SIG2
5


3V3 PLANE

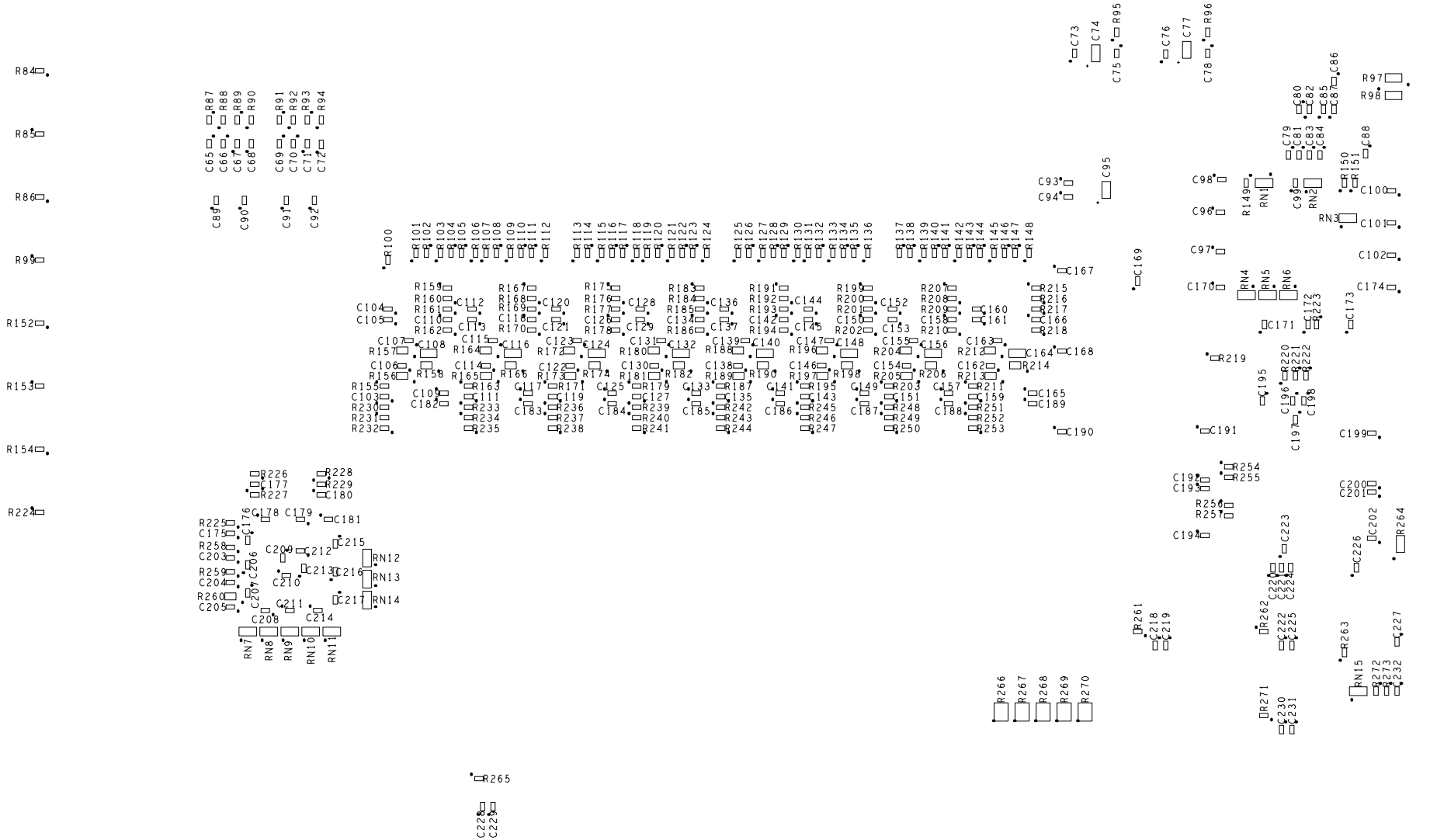
GND PLANE



BOTTOM LAYER



COMP BOTTOM



SILK BOTTOM

R84
R85
R86
R99
R152
R153
R154
R224
C65
C66
C67
C68
C69
C70
C71
C72
C89
C90
C91
C92
R87
R88
R89
R90
R91
R92
R93
R94
R100
R101
R102
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
R113
R114
R115
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R143
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R145
R146
R147
R148
C73
C74
C75
C76
C77
C78
R95
R96
C93
C94
C95
C169
C167
C168
C165
C189
C190
C79
C80
C81
C82
C83
C84
C85
C86
C87
R97
R98
R149
RN1
C98
C96
C97
C170
RN4
RN5
RN6
C171
R219
C191
C195
C196
C197
C198
R220
R221
R222
C173
C174
C223
C99
RN2
RN3
R150
R151
C88
C100
C101
C102
C199
C200
C201
C202
R264
C226
R263
C227
RN15
R272
R273
C232
C231
C230
R271
C220
C221
C222
C224
C225
R262
R254
R255
R256
R257
C192
C193
C194
C218
C219
R261
R266
R267
R268
R269
R270
C228
C229
R265
RN7
RN8
RN9
RN10
RN11
RN12
RN13
RN14
C205
C204
C203
C175
C176
C177
C178
C179
C180
C181
C206
C207
C208
C209
C210
C211
C212
C213
C214
C215
C216
C217
R260
R259
R258
R225
R226
R227
R228
R229

APPENDIX C: VHDL CODE FOR FPGA

```
-- ------------------------------------------------------------------
-- ------------------------------------------------------------------
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-- Tel: 604-415-6000
-- Fax: 604-415-6206
-- email: apps@pmc-sierra.com
-- ------------------------------------------------------------------
-- Project      : PMC-990354
-- File Name  : dslam_line_top.vhd
-- Path               :
-- Designer   : SW
--
-- Revision History
-- Issue       Date          Initials Description
-- 1           08/17/99      SW       Initial Release
-- 1.1         09/17/99      WT       debugging errors,
--                                    added comments
-- 1.2         11/03/99      WT       Added buffer components
--                                    changed internal fpga by
--                                    adding initialization on reset
--
-- Function
```

```
-- This is the top level of the VHDL code required for the DSLAM LINE
-- reference design.  The code creates some registers, does some muxing
-- for various timing options, supplies some glue logic for microprocessor
-- signals and acts as a buffer for the address and data bus.
--------------------------------------------------------------------



library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

library a42mx;

entity dslam_line_top is
        port (
        a_m : in std_logic_vector (23 downto 0);
        rwb_m : in std_logic;
        asb : in std_logic;
        dsb : in std_logic;
        siz0 : in std_logic;
        siz1 : in std_logic;
        cs0b : in std_logic;
        cs1b : in std_logic;
        cs2b : in std_logic;
        cs3b : in std_logic;
        d_m : inout std_logic_vector (7 downto 0);
        rsync : in std_logic_vector (15 downto 0);
        rx8k : in std_logic;
        mode : in std_logic;
        uweb : out std_logic;
        lweb : out std_logic;
        oeb : out std_logic;
        deb_mem : out std_logic;

        a_cometa : out std_logic_vector (8 downto 0);
        a_cometb : out std_logic_vector (8 downto 0);
        a : out std_logic_vector (7 downto 0);
        d_cometa : inout std_logic_vector (7 downto 0);
        d_cometb : inout std_logic_vector (7 downto 0);
        rdb : out std_logic;
        wrb : out std_logic;
        duplex_csb : out std_logic;
        tx8k : out std_logic;
        xclk_a : out std_logic;
```

```
        xclk_b : out std_logic;
        comet_led : out std_logic_vector (3 downto 0);
        tclki_a : out std_logic;
        tclki_b : out std_logic;
        d : inout std_logic_vector (7 downto 0);
        comet_csb : out std_logic_vector (15 downto 0);

        xclk_input : in std_logic;

        expansion_port1 : inout std_logic_vector (6 downto 0);
        expansion_port2 : inout std_logic_vector (6 downto 0);
        fpga1 : in std_logic;
        fpga2 : in std_logic;
        fpga3 : in std_logic;
        fpga4 : in std_logic
        );
end dslam_line_top;

architecture dslam_line_top_arch of dslam_line_top is

--
-- added by WT
-- buffer components added for A42MX36 specific layout problems
--
component BUFF
 port (A : in std_logic;
       Y : out std_logic
      );
end component;

type regtype is array (0 to 3) of std_logic_vector (7 downto 0);
signal fpga_reg : regtype;

--
-- added by WT
-- signals used by buffers to eliminate long horizontal tracks created in
-- device during layout
--
signal a_m_buff : std_logic_vector (8 downto 0);
signal d_m_buff : std_logic_vector (7 downto 0);

begin

--
-- This section is for the internal fpga registers used to control
```

```
-- the timing multiplexing functions
--

process (dsb, fpga4)
-- This process provides write ability to the internal fpga registers
-- The fpga is placed on chip select 2 of the microprocessor
-- The base address of the fpga registers are 0x1001 1000 (hex)
-- On reset to the board, the fpga registers are initialized to their
-- default value.
-- note fpga4 is tied to signal RESETB
-- fpga_reg(0) = tclk_a select = 2.048MHz = "00010000"
-- fpga_reg(1) = tclk_b select = 2.048MHz = "00010000"
-- fpga_reg(2) = tx8k select = COMET#0 RSYNC = "00000000"
-- fpga_reg(3) = comet_leds = OFF = "00000000"

        variable int: integer range 0 to 3 ;
begin
        if fpga4 = '0' then
                fpga_reg(0) <= "00010000";
                fpga_reg(1) <= "00010000";
                fpga_reg(2) <= "00000000";
                fpga_reg(3) <= "00000000";
        end if;
        if fpga4 = '1' then
                if (cs2b = '0') and (a_m(16 downto 12) = "11000") and (rwb_m = '0') and
(dsb = '0') then
                        int := to_integer(unsigned(a_m(1 downto 0)));
                        fpga_reg(int) <= d_m;
                end if;
        end if;
end process;

--
-- COMET #0 - #7 tclk select
--
tclki_a <= rsync(to_integer(unsigned(fpga_reg(0)))) when (fpga_reg(0)(7 downto 4) =
"0000")
           else rx8k when (fpga_reg(0)(4 downto 0) = "11111")
           else xclk_input;

--
-- COMET #8 - #15 tclk select
--
tclki_b <= rsync(to_integer(unsigned(fpga_reg(1)))) when (fpga_reg(1)(7 downto 4) =
"0000")
```

```
        else rx8k when (fpga_reg(1)(4 downto 0) = "11111")
        else xclk_input;

--
-- S/UNI-DUPLEX tx8k input select
--
tx8k <= rsync(to_integer(unsigned(fpga_reg(2)(3 downto 0))));

--
-- COMET Status LED control
--
comet_led <= fpga_reg(3)(3 downto 0);

--
-- COMET XCLK Buffer
--
xclk_a <= xclk_input;
xclk_b <= xclk_input;

--
-- This section added to help debug internal fpga registers
-- fpga3 is used as an debug enable '1' is enable '0' is highZ
--
process (fpga3, fpga_reg)
begin
        if fpga3 = '0' then
                expansion_port1 <= "ZZZZZZZ";
                expansion_port2 <= "ZZZZZZZ";
        end if;
        if fpga3 = '1' then
                expansion_port1 <= fpga_reg(0)(6 downto 0);
                expansion_port2 <= fpga_reg(1)(6 downto 0);
        end if;
end process;


--
-- This section is for the microprocessor glue logic signals
--
lweb <= not (((not siz0) or(a_m(0))) and (not cs1b) and (not rwb_m)) when mode = '1'
        else not (((not siz0) or(a_m(0))) and (not (cs1b and cs0b)) and (not rwb_m));

uweb <= not ((not rwb_m) and (not a_m(0)) and (not cs1b)) when mode = '1'
        else not ((not rwb_m) and (not a_m(0)) and (not (cs1b and cs0b)));
```

```
oeb <= not (rwb_m and (not cs1b)) when mode = '1'
      else not (rwb_m and (not (cs1b and cs0b)));

wrb <= rwb_m;
rdb <= not rwb_m;
deb_mem <= cs0b and cs1b;

--
-- This section is the address buffers
--
a_m_b0: BUFF port map (A => a_m(0), Y => a_m_buff(0));
a_m_b1: BUFF port map (A => a_m(1), Y => a_m_buff(1));
a_m_b2: BUFF port map (A => a_m(2), Y => a_m_buff(2));
a_m_b3: BUFF port map (A => a_m(3), Y => a_m_buff(3));
a_m_b4: BUFF port map (A => a_m(4), Y => a_m_buff(4));
a_m_b5: BUFF port map (A => a_m(5), Y => a_m_buff(5));
a_m_b6: BUFF port map (A => a_m(6), Y => a_m_buff(6));
a_m_b7: BUFF port map (A => a_m(7), Y => a_m_buff(7));
a_m_b8: BUFF port map (A => a_m(8), Y => a_m_buff(8));

a <= a_m_buff(7 downto 0);
a_cometa <= a_m_buff;
a_cometb <= a_m_buff;

--
-- This section is the data bus buffers
--
d_m_b0: BUFF port map (A => d_m(0), Y => d_m_buff(0));
d_m_b1: BUFF port map (A => d_m(1), Y => d_m_buff(1));
d_m_b2: BUFF port map (A => d_m(2), Y => d_m_buff(2));
d_m_b3: BUFF port map (A => d_m(3), Y => d_m_buff(3));
d_m_b4: BUFF port map (A => d_m(4), Y => d_m_buff(4));
d_m_b5: BUFF port map (A => d_m(5), Y => d_m_buff(5));
d_m_b6: BUFF port map (A => d_m(6), Y => d_m_buff(6));
d_m_b7: BUFF port map (A => d_m(7), Y => d_m_buff(7));

d_cometa <= d_m_buff when ((cs2b = '0') and (rwb_m = '0') and (a_m(16) = '0') and
(a_m(15) = '0'))
            else "ZZZZZZZZ";

d_cometb <= d_m_buff when ((cs2b = '0') and (rwb_m = '0') and (a_m(16) = '0') and
(a_m(15) = '1'))
            else "ZZZZZZZZ";
```

```
d <= d_m_buff when ((cs2b = '0') and (rwb_m = '0') and (a_m(16) = '1') and (a_m(15) =
'0'))
            else "ZZZZZZZZ";

d_m <= d_cometa when ((cs2b = '0') and (rwb_m = '1') and (a_m(16) = '0') and
(a_m(15) = '0')) else
      d_cometb when ((cs2b = '0') and (rwb_m = '1') and (a_m(16) = '0') and (a_m(15) =
'1')) else
      d       when ((cs2b = '0') and (rwb_m = '1') and (a_m(16) = '1') and (a_m(15) = '0'))
      else "ZZZZZZZZ";

--
-- This section is the chip select logic
--
comet_csb(0) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (not
a_m(14)) and (not a_m(13)) and (not a_m(12)));

comet_csb(1) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (not
a_m(14)) and (not a_m(13)) and (    a_m(12)));

comet_csb(2) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (not
a_m(14)) and (    a_m(13)) and (not a_m(12)));

comet_csb(3) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (not
a_m(14)) and (    a_m(13)) and (    a_m(12)));

comet_csb(4) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (    a_m(14))
and (not a_m(13)) and (not a_m(12)));

comet_csb(5) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (    a_m(14))
and (not a_m(13)) and (    a_m(12)));

comet_csb(6) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (    a_m(14))
and (    a_m(13)) and (not a_m(12)));

comet_csb(7) <= not ((not cs2b) and (not a_m(16)) and (not a_m(15)) and (    a_m(14))
and (    a_m(13)) and (    a_m(12)));

comet_csb(8) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (not a_m(14))
and (not a_m(13)) and (not a_m(12)));

comet_csb(9) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (not a_m(14))
and (not a_m(13)) and (    a_m(12)));
```

```
comet_csb(10) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (not
a_m(14)) and (    a_m(13)) and (not a_m(12)));

comet_csb(11) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (not
a_m(14)) and (    a_m(13)) and (    a_m(12)));

comet_csb(12) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (    a_m(14))
and (not a_m(13)) and (not a_m(12)));

comet_csb(13) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (    a_m(14))
and (not a_m(13)) and (    a_m(12)));

comet_csb(14) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (    a_m(14))
and (    a_m(13)) and (not a_m(12)));

comet_csb(15) <= not ((not cs2b) and (not a_m(16)) and (    a_m(15)) and (    a_m(14))
and (    a_m(13)) and (    a_m(12)));

duplex_csb    <= not ((not cs2b) and (    a_m(16)) and (not a_m(15)) and (not a_m(14))
and (not a_m(13)) and (not a_m(12)));

end dslam_line_top_arch;
```

APPENDIX D: BILL OF MATERIALS

This table shows the materials needed to assemble the Line Card.

Table 8 - Bill of Materials

Item	Description	Vendor Part Number	Reference Designator	Qty
1	1N5817_-1N5817M	1N5817M	D5	1
2	74F08_SOIC-BASE	74F08	U65	1
3	74FCT16245_1_SSOP48- BASE	74FCT16245T	U42	1
4	74FCT245_1_SOIC20W-BASE	74FCT245T	U43, U44, U62	3
5	A42MX36_PQ208_SOCKET 2-BASE	A42MX36_PQ208 & YAMAICHI IC149-208-0	U61	1
6	AT27C4096_PLCC-100NS	AT27C4096-10JI	U37	1
7	BANTAM-BASE	ELECTRO SONIC -- PC-834-J-(BLACK)	J6-J8, J17, J20-J22, J24	8
8	CAPACITOR-0.01UF, 50V, X7R_603	DIGIKEY PCC103BVCT-ND	C103, C105-C107, C109-C111, C113-C115, C117-C119, C121-C123, C125-C127, C129-C131, C133-C135, C137-C139, C141-C143, C145-C147, C149-C152, C154, C155, C157-C159, C161-C163, C165, C166, C175, C176, C181, C203-C205, C207, C209, C211, C213, C215, C217, C218, C225, C229, C231	64
9	CAPACITOR-0.1UF, 16V, X7R_603	PANASONIC -- ECJ-1VB1C104K	C1, C48, C49, C55, C56, C58, C59, C63, C73, C75, C76, C78-C94, C96-C102, C104, C112, C120, C128, C136, C144, C153, C160, C167-C174, C177-C180, C182-C202, C206, C208, C210, C212, C214, C216, C219-C224, C226-C228, C230, C232	93

Item	Description	Vendor Part Number	Reference Designator	Qty
10	CAPACITOR-0.22UF, 10V, X7R_603	DIGI-KEY -- PCC1749CT-ND	C65-C72	8
11	CAPACITOR-0.33UF, 35V, TANT TEH	DIGI-KEY -- PCT6334CT-ND	C61	1
12	CAPACITOR-1000UF, 10V, ELECTRO_SA	DIGI-KEY -- PCE3178CT-ND	C62	1
13	CAPACITOR-10UF, 16V, TANT TEH	DIGI-KEY -- PCT3106CT-ND	C43, C44, C64	3
14	CAPACITOR-10UF, 6.3V, TANT TE	DIGI-KEY -- PCS1106CT-ND	C2, C74, C77, C95	4
15	CAPACITOR-1UF, 16V, TANT TEH	DIGI-KEY -- PCT3105CT-ND	C54, C108, C116, C124, C132, C140, C148, C156, C164	9
16	CAPACITOR-22UF, 16V, TANT TEH	DIGI-KEY -- PCT3226CT-ND	C3, C36-C42, C46, C47	10
17	CAPACITOR-22UF, 6.3V, TANT TEH	DIGI-KEY -- PCT1226CT-ND	C7, C11, C15, C19, C23, C27, C31, C35, C45, C50-C52	12
18	CAPACITOR-4.7UF, 10V, TANT TEH	DIGI-KEY -- PCT2475CT-ND	C4, C6, C8, C10, C12, C14, C16, C17, C20, C21, C24, C25, C28, C29, C32, C33	16
19	CAPACITOR-4.7UF, 16V, TANT TEH	DIGI-KEY -- PCT3475CT-ND	C57, C60	2
20	CAPACITOR-47UF, 10V, TANT TEH	DIGI-KEY -- PCT2476CT-ND	C53	1
21	CAPACITOR-68UF, 6.3V, TANT TEH	DIGI-KEY -- PCT1686CT-ND	C5, C9, C13, C18, C22, C26, C30, C34	8
22	COMET_CABGA-BASE	PM4351-NI	U45-U60	16
23	CONN160_71626-4000-B ASE-GND=CHA	MOLEX -- 71626-4000	P2	1
24	CONN160_MALE_71624-2 004-BASE-GA	MOLEX -- 71624-2004	P3	1
25	CPCI_ESD_STRIP_BOTTO M_EDGE-BASE	PART OF PCB	P1	1
26	CY7C1049-25NS	CY7C1049L-25VC	U2, U3	2

Item	Description	Vendor Part Number	Reference Designator	Qty
27	DI9410_SOIC-BASE	DI9410	Q2	1
28	DIODE_SCHOTTKY_ SMB_2 -2A, 20V	DIGI-KEY -- B220DICT-ND	D4	1
29	H1026_SMD-BASE	H1026	T5	1
30	HEADER2_100 MIL-BASE	DIGI-KEY S1011-36-ND	J25	1
31	HEADER2_JUMPER-BASE	DIGI-KEY S1011-36-ND	J19	1
32	HEADER3S-BASE	DIGI-KEY S1011-36-ND	J9-J16	8
33	HEADER4-BASE	DIGI-KEY S1011-36-ND	J18	1
34	HEADER5X2-BASE	DIGI-KEY S2012-36-ND	J3	1
35	HEADER5_100 MIL-BASE	DIGI-KEY S1011-36-ND	J23	1
36	HEADER6_100 MIL-BASE	DIGI-KEY S1011-36-ND	J27	1
37	HEADER_8X2-BASE	HEADER_8X2	J26	1
38	LC03_6_SOIC-BASE	LC03_6	U4-U35	32
39	LT1585_TO-220_HORZ-B ASE	LT1585CT-3.3	U68	1
40	LTC1422_SOIC-BASE	LTC1422CS8	U67	1
41	MAX202_1_SOIC16-BASE	MAX202CSA	U1	1
42	MC68340_1	MOTOROLA MC68340	U36	1
43	MMBT3904	MMBT3904	Q1	1
44	MOLEX53460_0611_2 MM- BASE	53460-0611	J4, J28	2
45	MOUNTING_HOLE-150 MIL	PART OF PCB	M2	1
46	OSC_4PIN_25.0000M HZ- BASE	DIGIKEY CTS CTX171-ND	Y2	1

Item	Description	Vendor Part Number	Reference Designator	Qty
47	OSC_4PIN_3.6864MHZ-B ASE	DIGIKEY CTS CTX154-ND	Y3	1
48	OSC_TTL_DIP-2.048MHZ , 50 PPM, CHA	K1150BA	Y1	1
49	OSC_TTL_DIP-25.0000M HZ, 100 PPMA	DIGI-KEY -- CTX176-ND	Y4	1
50	PBNO_VERT_6MM-BASE	DIGIKEY -- P8009S-ND	SW1, SW2	2
51	PWRBLOCK_2-BASE	TERMINAL BLOCK	P4	1
52	RESISTOR-.01, 1%, 1206	IRC-TT LRC-LR1206-01-R01 0-F	R44	1
53	RESISTOR-.10, 5%, 1210	IRC-TT LRC-LR1210-01-R10 0-F	R37, R41-R43, R45, R266-R270	10
54	RESISTOR-.47, 1%, 805	DIGI-KEY -- P<VALUE>DCT-ND	R13-R20	8
55	RESISTOR-0, 5%, 805	DIGI-KEY -- P<VALUE>ACT-ND	R30-R33	4
56	RESISTOR-1.0, 5%, 805	DIGI-KEY -- P<VALUE>BCT-ND	R156, R157, R164, R165, R172, R173, R180, R181, R188, R189, R196, R197, R204, R205, R212, R213	16
57	RESISTOR-1.00M, 1%, 603	DIGI-KEY -- P<VALUE>MHCT-ND	R87-R94	8
58	RESISTOR-1.0K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R50, R51, R56, R57, R62, R63, R68, R69, R75, R78, R80, R81, R222, R225	14
59	RESISTOR-10, 5%, 603	DIGI-KEY -- P10GCT-ND	R38	1
60	RESISTOR-100, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R1-R4, R11, R49, R52, R55, R58, R61, R64, R67, R70, R73, R76, R79, R82, R84-R86, R99, R152-R154, R224	25

Item	Description	Vendor Part Number	Reference Designator	Qty
61	RESISTOR-100K, 5%, 603	DIGI-KEY -- P100KGCT-ND	R100, R161, R169, R177, R185, R193, R201, R209, R217, R230, R233, R236, R239, R242, R245, R248, R251	17
62	RESISTOR-10K, 1%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R219, R263	2
63	RESISTOR-10M, 5%, 1206	DIGI-KEY -- P<VALUE>ECT-ND	R97, R98, R264	3
64	RESISTOR-12.7, 1%, 603	DIGI-KEY -- P12.7HCT-ND	R102, R103, R105, R106, R108, R109, R111, R112, R114, R115, R117, R118, R120, R121, R123, R124, R126, R127, R129, R130, R132, R133, R135, R136, R138, R139, R141, R142, R144, R145, R147, R148	32
65	RESISTOR-18.2, 1%, 603	DIGI-KEY -- P18.2HCT-ND	R101, R104, R107, R110, R113, R116, R119, R122, R125, R128, R131, R134, R137, R140, R143, R146	16
66	RESISTOR-2.0K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R47, R53, R54, R59, R60, R65, R66, R71, R72, R74, R77, R83	12
67	RESISTOR-2.2, 1%, 805	DIGI-KEY -- P<VALUE>DCT-ND	R158, R166, R174, R182, R190, R198, R206, R214	8
68	RESISTOR-2.43K, 1%, 603	DIGI-KEY -- P<VALUE>HCT-ND	R39	1
69	RESISTOR-20.0, 1%, 603	DIGI-KEY -- P20.0HCT-ND	R258, R259	2
70	RESISTOR-200, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R46, R48	2
71	RESISTOR-270, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R5-R10, R12	7
72	RESISTOR-3.3, 1%, 805	DIGI-KEY -- P<VALUE>DCT-ND	R260	1
73	RESISTOR-33, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R220, R221	2
74	RESISTOR-4.75K, 1%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R21	1

Item	Description	Vendor Part Number	Reference Designator	Qty
75	RESISTOR-4.7K, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R22, R27-R29, R34-R36, R95, R96, R149-R151, R159, R167, R175, R183, R191, R199, R207, R215, R223, R232, R235, R238, R241, R244, R247, R250, R253, R272, R273	31
76	RESISTOR-430, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R227, R228	2
77	RESISTOR-49.9, 1%, 603	DIGI-KEY – P49.9HCT-ND	R23-R26	4
78	RESISTOR-56, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R155, R160, R162, R163, R168, R170, R171, R176, R178, R179, R184, R186, R187, R192, R194, R195, R200, R202, R203, R208, R210, R211, R216, R218, R231, R234, R237, R240, R243, R246, R249, R252, R254-R257, R261, R262, R265, R271	40
79	RESISTOR-6.81K, 1%, 603	DIGI-KEY -- P6.81KHCT-ND	R40	1
80	RESISTOR-750, 5%, 603	DIGI-KEY -- P<VALUE>GCT-ND	R226, R229	2
81	RES_ARRAY_4_SMD-4.7K	DIGI-KEY -- Y4<VALUE CODE>-ND	RN1-RN6, RN15	7
82	RES_ARRAY_4_SMD-56	DIGI-KEY -- Y4<VALUE CODE>-ND	RN7-RN14	8
83	RJ45-BASE	RJ45	J2	1
84	SSF_LXH5147-LGD	SSF-LXH5147LGD	D3	1
85	SSF_LXH5147-LID	SSF-LXH5147LID	D1, D2	2
86	SUNIDUPLEX_SERIAL_PB GA-BASE	PM7350-PI	U64	1
87	T9021_-BASE	T9021	U38-U41	4
88	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP7	1

Item	Description	Vendor Part Number	Reference Designator	Qty
89	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP8, TP15, TP18, TP23	4
90	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP3, TP10, TP16, TP25	4
91	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP1, TP6	2
92	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP2	1
93	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP12	1
94	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP13	1
95	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP9	1
96	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP20	1
97	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP4, TP5, TP11, TP14, TP17, TP21, TP22, TP24, TP26	9
98	TST_PT-BASE	DIGI-KEY S1011-36-ND	TP19	1
99	ZPACK5X22FH_ASCPCI_2 MM	352068-1	J1	1
100	ZPACK5X22FH_BSCPI_2M M	352152-1	J5	1

NOTES

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